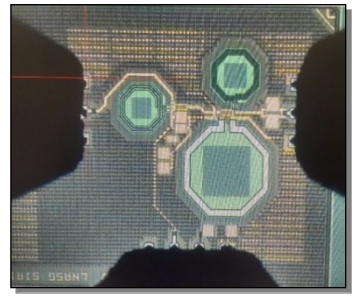
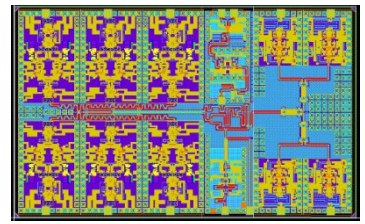
Technology Field 1: Energy Efficient Chips

Summary of achievements at TF level

IPCEI created substancial progress on Energy Efficient Chips manufactured in Europe – all along the value chain

- Exploring new substrates, material solutions and add-on functionalities for ultra-low power technology platforms
- Developing the maturity of those ultra-low power technology platforms in the FID phase
- Increasing the offer of these platforms with new functionalities and a whole design ecosystem
- Facilitating the access for SMEs and Universities
- Increasing the market take-up of these technologies for a Green Deal compatible digital transformation
- Creating new infrastructures and industrial jobs in Europe
- Serving society with new digital solutions





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CEA-Leti - Improvement of the FDSOI-based transistor performance (performance boosters)
Continuation of the investigation of OxRAM and Mott memories with STM.
In collaboration with SOITEC: Start of the 300mm pilot fine for the R&D of new SOI substrates and technologies

Cologne Chip succeeded in development and production of the first and only European FPGA. The GateMate(TM) FPGA is now available for developers, design houses and customers.

GlobalFoundries – completed RDI phases of 10 technology variants of 22FDX . Further RDI included functional enhancements for 22FDX, like security devices or optical elements, important knowhow to extend or secure operability of 22FDX, Design-IP elements, Design enablement for lowest operating voltages <0.6V as well as demonstrators for 5G, auto-radar and imaging radar & a new green & sustainable system demonstrator with world record in energy efficiency. IPCEI involved more than 400 engineers directly at GF and another 120 at subcontracts. Assuming customers convert their chips from 40 to 22nm technology and operate 2h/day, 5.1 Megatons CO_2 can be saved per year based on GF's production volume in Dresden. Further 0.6 Megatons per year could be saved by using the backbias function of 22FDX. This describes IPCEI WIN-FDSOI's impact to the European Green Deal, possible energy savings by digital transformation & its contribution to climate targets.

NXP – Implementation of hardware-based security concept for energy efficient and trustworthy EBS solutions has progressed well in 2021 despite significant technical challenges. Engineering samples are in preparation, and FID phase has already started. Significant dissemination and spill-over activities executed in 2021 (example: ECSEL Austria conference – picture at the right).

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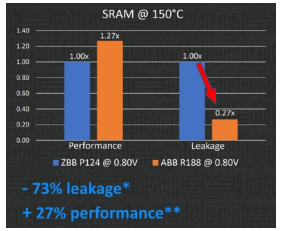
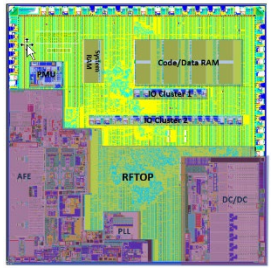
RacyICs – developed contributions to its ABX Adaptive Body Biasing Platform comprising std cells, SRAM, IO and other components. Demonstrated unparalleled power-efficiency as well as power/performance/area for IoT devices.
Developed embedded FPGA, power management, and analog IP for an IoT platform solution.



Soitec –developed its second generation of 300mm FD-SOI substrates for nodes beyond 22nm, 300mm RF-SOI substrates for 5G and disruptive 150mm POI (Piezo on Insulator) substrates family for smartphone RF filters developed. These developments induced the conversion of a 300mm SOI Fab, a 150mm plant dedicated to POI and generated more than 400 highly qualified jobs. Our innovative substrates contribute to Green Deal objectives by enabling performant and energy efficient semiconductors technologies. Thanks to IPCEI and spillover the European ecsosytem using these technologies has been considerably increased along the Value chain

STMicroelectronics – developed new functionalities on the ultra low power 28nm FDSOI: Fully integrated 60GHz radio circuit and antenna, 16Mb Phase Change Memory, 77GHz radar sensors for automotive. The RF-SOI technology was developed in 65nm node and the 350GHz range was achieved proving the validity of this technology for the MMW frequency range. Developments of automotive MCUs in 40nm CMOS.



XFAB – developed wafer level 3D assembly of GaN on RF-SOI for RF applications. Concurrent RF/mmW design flow methodologies were established and implemented for 3D heterogeneous concepts, as well as Design methodologies for process yield optimization.