Challenges and capabilities of 3D integration in CMOS imaging sensors

Dominique Thomas, Jean Michailos, Krysten Rochereau
Joris Jourdon, Sandrine Lhostis
STMicroelectronics, France
dominique.thomas@st.com

September 23-26, 2019
Outline

- 3D Integration principles
- 3D Integration for imagers
- Hybrid bonding for imagers demonstration
- Fine pitch Hybrid bonding
  - Issues and demonstration
- Future directions
3D-Integration: principle

- New system design paradigm: 3D partitioning
- Key technological benefits:
  - Reduction of interconnects lengths RC delay decrease
  - Heterogeneous integration
  - Density vs form factor
3D-Stacked Image sensors

- Form factor improvement
- Optimized process dedicated to each silicon layer
- Area in the logic die available for added value
  - Great interest of 3D integration for image sensors
Different integration schemes have been developed specifically for the CMOS Image Sensor (CIS) market.
What is Hybrid Bonding (HB)?

- Face to face interconnections
  - Double Damascene Copper stack between top chip last metal and bottom chip last metal.
  - Pitch ≤ 10µm
Morphology

- No glue but molecular bonding
  - Direct SiO2/SiO2 bonding: SiOH-SiOH $\rightarrow$ Si-O-Si
  - At Cu-Cu interface: grain growth/migration by anneal
3D HB-stacked imager demo

- First Generation
  - Pixel 1.5 µm
  - Bonding pitch 9.3 µm

- But...

- High density BH (~1 µm) will
  - Reduce footprint
  - Allow pixel-level optimization

<table>
<thead>
<tr>
<th>Resolution</th>
<th>14MPix, 4640 x 3056</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>1.53µm x 1.53µm</td>
</tr>
<tr>
<td>Technology</td>
<td>ST 3D stack</td>
</tr>
<tr>
<td></td>
<td>IMG3D BSI</td>
</tr>
<tr>
<td></td>
<td>CMOS40LP</td>
</tr>
<tr>
<td>Optical Format</td>
<td>1/2.3&quot; (diagonal of 7.75mm)</td>
</tr>
</tbody>
</table>

Computer Vision system:
- Face identification
- Gender identification
- Age estimation
- Happiness estimation
- ...
Fine pitch Interconnect

7.2 µm

1.44 µm

- Pitch shrinkage ➔
- Opportunity of new pixel architecture
Hybrid bonding process flow

- **Bonding pad + vias dual-damascene**
- **Bonding at room temperature**
- **Bonding annealing at 400 °C**

**TOP**
- Copper
- SiO$_2$
- Diffusion barrier
- Capping

**BOTTOM**

S. Lhostis, ECTC, 2016
Fine pitch Intconnects’ challenges

Process

Yield
Overlay
Electromigration
Delamination
Copper diffusion

Reliability

V− V
Resistance measurement of 30k interconnects daisy chains
- Yield not affected by the 5x reduction of bonding pitch
- Tool alignment capability (200 nm @ +/- 3σ) is sufficient
Delamination (stress)

- Fine pitch → Higher average stress: a priori higher risk of delamination
- -55°C/+150 °C 500 cycles → Results: resistance well within specifications
- Electromigration was also tested (not shown here): → Results OK
The image quality is not degraded by going to finer wafer to wafer interconnection pitch.
Sequential Stacking: smaller pitch

**Parallel integration (Hybrid Bonding)**

1/ Wafers separately processed
2/ Stacking and contacting

**Sequential integration (Monolithic)**

1/ Bottom device processing (Photodiode or Transistor)
2/ Bonding Tier1 to Tier2 (SOI stack)
3/ Top MOSFET processing
4/ Contacting

**Limited by Bonder Align performances**
$\sigma_{//} \sim 200\text{nm}$
Challenging
Unlimited $T^\circ\text{C}$

**Alignment performance**
Contact process
Top layer thermal budget

**Sequential performance**
$\sigma_{SEQ} \sim 10\text{nm}$
Planar scheme like
~ Limited $T^\circ\text{C}$

**FE litho-like limited by Scanner**
Further steps: 3 layers

Source LETI/IRT

Oxide-Oxide DIRECT Bonding + TSV

Sony ISSCC 2017 and TechInsights May 2017
CONCLUSION

- 3D Integration is a powerful tool to increase imaging sensors capabilities

- Hybrid Bonding allows μm scale device to device interconnect
  - Permitting pixel level contacts improvement
  - Preliminary electrical and reliability show industrial viability

- Further work include
  - Fully exploring the capabilities ans limitations of fine pitch Hybrid bonding
  - Pitch reduction using sequential stacking: allows deep pixel 3D architecture exploration
  - Adding more layers for system integration

D. Thomas
ESSDERC 2019 IPCEI on microelectronics focus session
Include Key References