Current SiC Power Device Development, Material Defect Measurements and Characterization at Bosch

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***Abstract*—This paper consists of two parts, where the first gives an overview of current power device development on 150 mm 4H silicon carbide (SiC) taking place at Robert Bosch GmbH in Reutlingen. The general process flow is explained and its separation in three distinctive groups, i.e. trench etched metal-oxide semiconductor (Trench-MOS) fabrication, ion implantation and metallization, is motivated. A brief overview, as well as a deeper explanation of three of the most important processes concerning wafer quality for SiC MOS field-effect transistor (MOSFET) power device development is given. These processes include epitaxy, high temperature oxidation, ion implantation, as well as activation of implanted ions. It is also highlighted why established methods and respectively equipment available through previous development and ongoing silicon production can only be used partially.**
The second part describes the influence of diverse processes on the SiC surface morphology and intrinsic crystal structure. A non-destructive 4H-SiC material characterization method is used for defect analysis in SiC substrates and epitaxial layers. The method at hand for SiC defect detection connects confocal microscopy and ultra-violet photo-luminescence (UV-PL) scanning.
These defect measurement methods allow for both a characterization and classification of a wide range of different surface and intrinsic defects respectively in SiC wafer. During these material defect investigations we focus on intrinsic basal-plane dislocations (BPDs), as well as on different types of stacking faults (SFs) and triangular defects.

***Index Terms*—Bosch, Defect characterization, Epitaxy, High Temperature Activation, Ion Implantation, Power Devices, Trench-MOSFET, UV-PL, 150 mm, 4H-SiC.**

I. Introduction

The ongoing and increasing interest in the development of devices using silicon carbide (SiC) is not only warranted by the fact that the material is a wide bandgap semiconductor (E_{gap} = 3.268 eV) [1], [2] with a high electrical breakdown field of 2.5 MV/cm [3] and significantly lower switching losses compared to silicon devices, but also a high thermal conductivity (Θ_K = 4.9 W/cmK) which allows for smaller packaging as well as high power and temperature devices [1], [3].
Ambitious European endeavours (e.g. the Important Project of Common European Interest (IPCEI)) which for example attempt to find solutions for alternative means of transportation compared to fossil fuels coupled with the aforementioned superior material properties with regard to Si justify the increasing interest in SiC devices [1].

II. Overview of current SiC development

The development process of any silicon carbide (SiC) trench device consists of several distinct steps, which can be grouped into four major blocks. First the epitaxial layer grown, then the ion implantation process block, followed by Trench-MOS fabrication and metallization.
Fig. 1 shows a compact flowchart of the general workflow in SiC power device development. A precise description of all included steps would go beyond the framework of this paper and therefore three process steps, highlighted in Fig 1, which have a significant impact on surface and crystal defects, will be discussed in more detail. These include epitaxial layer growth, ion implantation as well as high temperature activation and annealing [4].

The fabrication of a SiC power device starts, after initial marking, cleaning and substrate characterization, with homo-epitaxial growth on a commercially available 150 mm 4H-SiC, 4° off-cut to the (0001) direction, substrate wafer. For this process the method of chemical vapour deposition (CVD), e.g. in a hot or warm-wall (planetary) reactor, is widely used [5]–[7].
The parameters with the biggest impact on electrical properties, e.g. blocking voltage, leakage currents or device degradation, of SiC devices are epitaxial layer thickness, doping type, i.e. n- or p-type, and uniformity as well as the number and type of surface and crystal defects [5]. For SiC epitaxy important parameters are temperature, carbon to silicon (C/Si) ratio, total gas flow and process pressure. At growth temperatures between 1500 °C and 1700 °C quartz cannot be used for reactor parts and new materials like SiC or TaC coated graphite have to be used.
On top of the difference in physical conditions a completely separate chemistry is used during the SiC growth process [8]. Therefore defect free epitaxy promises to be a challenging

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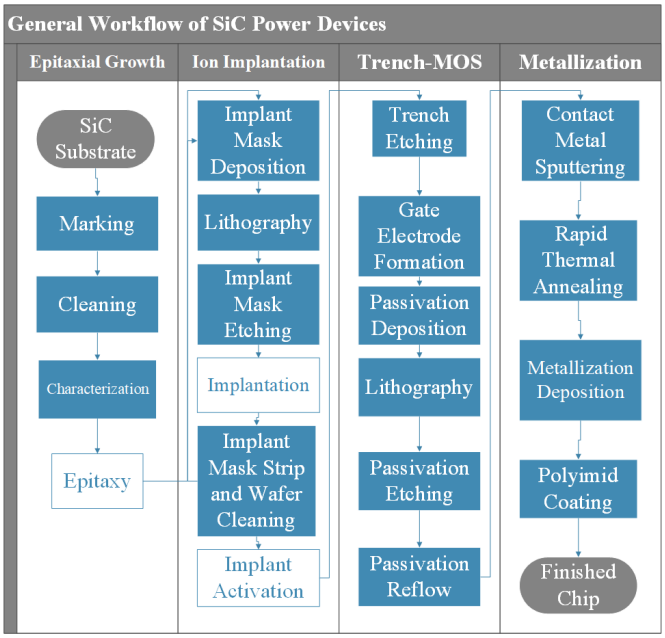

Fig. 1. Illustration of a typical process flow for SiC power Trench-MOSFET fabrication.

field in SiC high power device development [9].

Following the epitaxial layer growth, SiC wafers are implanted using accelerated ions to define the differently doped areas within the epitaxial layer. Since doping needs to be separated laterally, different hard masks need to be deposited, lithographed and etched prior to implantation. For mask deposition, photolithography and etching, semiconductor-industry standard equipment can be used but typically needs to be upgraded to handle optical transparent SiC substrates. Vapour deposition processes are preferred to thermal oxidation for the fabrication of ion implantation masks due to the very small oxidation rate of SiC. Depending on the required step coverage and the equipment available, different deposition processes can be used. For instance, low pressure chemical vapour deposition (LPCVD) can produce conformal silicon dioxide, silicon nitride or polysilicon layers at temperatures up to 1200 °C and pressures around 500 mBar [10]–[12]. In contrast, plasma-enhanced chemical vapour deposition (PECVD) can be used to grow thick mask layers at a process temperature of around 400 °C and a pressure of several mBar, with less step coverage and only as a single wafer process [10], [12], [13].
In contrast to substrate and epitaxial layer growth, where dopants are introduced during the growth process, selective doping of SiC is carried out by ion implantation. The implantation energy is directly proportional to the penetration depth of the ion beam, where typically up to several MeV are required for the fabrication of SiC Trench-MOS devices, and therefore to the characteristics of the device. A more exhaustive description of the ion implantation process in 4H-SiC can be found elsewhere [14].
For different devices different types of doping, i.e. n- and p-type, in distinct regions are necessary. To achieve various doping types during ion implantation several elements such as Al or B for p- and N or P for n-type are used, but not all are equally well suited for SiC [15], [16]. Since nitrogen is a gaseous precursor the necessary ion beam can be directly produced. This is not the case for the aluminium ion beam, where solid AlI_3 has to be vaporized and subsequently the gas ionized before it can be accelerated and used for p-type implantation [15].
Ion implantation by definition changes the surface morphology. A possible way to reduce the impact of implantation is to heat the wafer up to 600 °C during ion exposition, therefore resulting in a light annealing which reduces the impact of the implantation process on the surface and crystal structure [16]. Post implantation annealing is commonly used to decreases surface roughness of the wafer after ion implantation processes as well as activate the implanted dopants [16]. The annealing is carried out at high temperatures between 1700 °C and 2100 °C [16]. Although it is not possible to eliminate every surface defect introduced by implantation [15].
High temperature oxidation and activation is not only useful to improve the surface roughness, but also allows the implanted dopants simultaneously to diffuse into the SiC layers which therefore activates them electrically and is therefore indispensable for proper device performance. At these high temperatures any device structures start to soften slightly which has to be considered in the development of the annealing process. Donor atoms are fully activated at a temperature of 1500 °C, while acceptor atoms only activate fully at approximately 1600 °C [15].
According to Fig. 1, Trench-MOSFET fabrication follows the second block, beginning with gate trench plasma etching and MOS electrode formation. Subsequently, the passivation layer is deposited on the Trench-MOS electrode and lithographed. Finally, plasma etching is used to structure the passivation layer, followed by a shape-rounding passivation reflow process. [10]
The last and fourth block for SiC power device production forms silicide-based ohmic contacts to the previously produced semiconductor structure. Therefore, contact metal deposition is carried out by sputtering different elements, e.g. Ni, Ti, or Al. As previously discussed, SiC is a chemically stable material [1] with a large band gap and therefore requires a rapid thermal annealing step at around 1000 °C to form ohmic contacts between the subsequently deposited power metal stack and the SiC surface [10], [17]. This rapid thermal treatment is followed by sputtering of different metallic layers to form the so-called power metal stack. The sputtered metal layers are chosen in accordance to the advanced interconnection technology used in the following [10].

III. Defect Characterization

Up to this point it is not possible to create perfect, defect free 4H-SiC substrate wafers and subsequentially epitaxial layers. Dislocation densities of commercially available 150 mm substrate wafers are still in the range of >3000 cm^{-2}

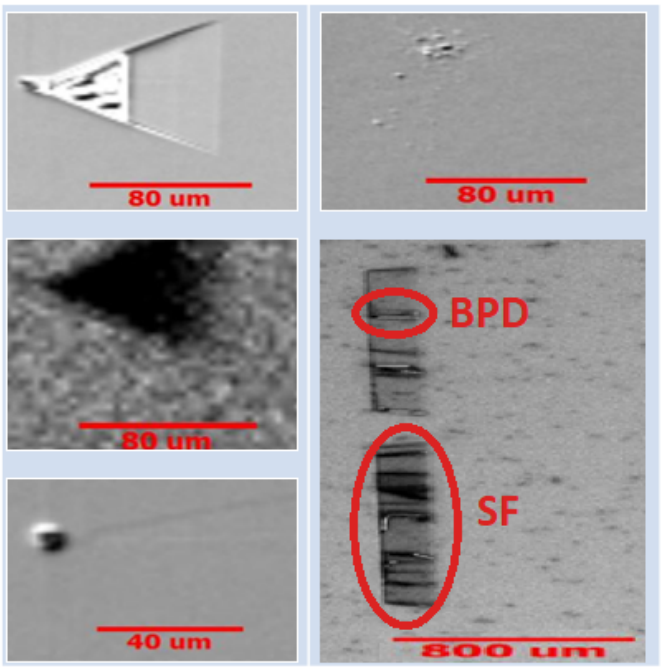

Fig. 2. Overview of common surface and crystal defects in SiC. Left top to bottom: Triangle defect on the wafer surface, PL triangle and particle downfall. Right top to bottom: A micro-pipe cluster, basal plane dislocations and bar shaped stacking faults.

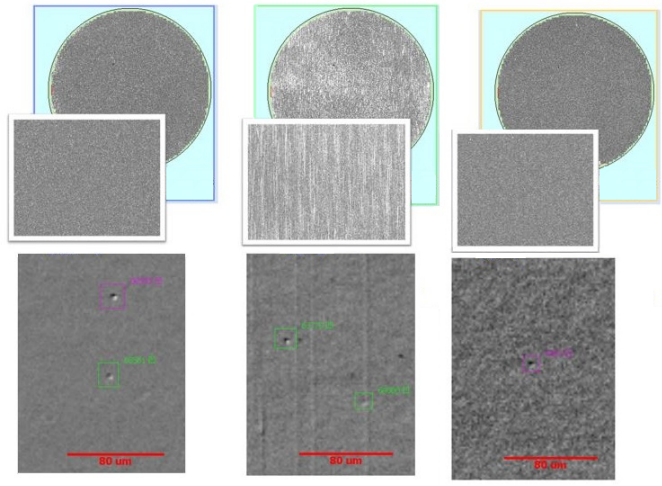

Fig. 3. Top: Surface roughness maps for three different wafer suppliers. Bottom: Enhanced sections of VIS measurements of the three different wafer suppliers. A difference in contrast and overall defect detection is visible.

[18]. Common SiC surface and crystal defects are shown in Fig. 2 [2]. These defects include triangles, particle downfalls, micro pipe clusters, basal plane dislocations (BPDs) and bar shaped stacking faults (SFs) [1], [2], [7]. Although many defects originate during crystal growth, like e.g. micro pies and carbon inclusions, which therefore can only be influenced during the substrate production, it is possible to transform defects into other types, e.g. basal plane dislocations into threading dislocations. [2] For these defect transformations significant energies and temperatures are necessary and therefore can only occur at certain steps in the device development process. These steps include epitaxial layer growth and high temperature oxidation, annealing and activation processes [2]. The generation of new defects is also possible e.g during high energy ion implantation. Part of the ongoing SiC power device development focuses on the questions which process steps influence defects and in which way.

Not only the origin and transformation potential of defects is variable, but also their influence on device performance. Triangular defects, micro pipes and downfalls are known to have a significant impact on the device regardless of the type. They are likely to cause leakage currents, degradation and overall device failure [2], [7]. Other defect types, like BPDs, in-grown stacking faults or threading dislocations can also influence device performance, but there impact is depending on the device structure, e.g. SBD, JFET or Trench-MOS [19]. Therefore significant development effort went into the reduction of these so called ”critical” defects to values of less than 0.1 cm^{-2} during crystal growth, but many other surface and crystal defects are still present and their behaviour as well as their influence on device performance is to be investigated [2].

A confocal microscope enhanced with differential interferometry contrast (DIC) techniques for the visible (VIS) spectrum, as well as ultra-violet photo-luminescence (UV-PL) spectroscopy with variable wavelengths between 300 nm and 500 nm for the intrinsic faults are used to measure surface morphology and crystal defects, as shown in Fig. 2.

Many surface defects show a signal in both the visible and photo-luminescence spectrum, e.g. downfalls, bumps and triangles, while the opposite is generally not the case [2]. Photo-luminescence measurements allow intrinsic characterization of the substrate and epitaxial layers which included triangular defects, plane dislocations and stacking faults [19]. Since the amount of BPDs and SFs on commercially available SiC substrates is still high and their impact on device performance not yet fully understood compared to critical defects, these defects are the most important ones for investigation. Another challenge of SF characterization occurs due to different SFs consisting of several distinct defect types, which have a distinguishable peak in their PL spectrum at respective wavelengths [19]. Therefore it is not possible to distinguish different SFs simultaneously with the tool at hand. For this reason stacking faults are still part of future investigations.

Another part of the analysis focuses on the difference between various SiC wafer suppliers. In the top part of Fig. 3 surface roughness maps of three different suppliers are shown. A difference in contrast and roughness, i.e. thickness uniformity, is clearly visible. This contrast variation leads to difficulties in the defect detection software, which results in different defect detection rates as shown in the bottom part of Fig. 3. In addition to this contrast variation different suppliers show a significant difference in the overall amount of defect

types. The sum of defects are comparable for two suppliers, while it was significantly lower for the third one. Not only the overall amount but also the type of detected defects varies significantly between the suppliers, e.g. many bumps or many pits. Therefore the optimisation of a correct detection and classification of defects is still under investigation.

IV. Conclusion

The first part of this paper showcased the general workflow for SiC high power devices at Robert Bosch GmbH, starting with substrate wafer marking and characterization and ending with metal sputtering and polyimid coating, and gave insight why this technology proves to be a challenging field of development with several new challenges compared to established silicon semiconductor device process flows. Furthermore three processes, epitaxial layer growth, ion implantation and high temperature activation and annealing were described in more detail as well as their influence on SiC wafer surface morphology and intrinsic crystal defects outlined.
The second part lists typical SiC substrate and epitaxial layer defects, e.g. triangles, micro pipe clusters, basal plane dislocations or bar shaped stacking faults. It is summarized where they can be generated and possible conversion steps and influences from other power device processes, e.g. during epitaxial layer growth and other high temperature or energy process steps. Additionally the influence of defects on electrical device performance, e.g. leakage currents or device degradation is mentioned and a motivation behind the focus on basal plane dislocations and bar shaped stacking faults as well as conversion mechanism is given.

V. Outlook

Future investigations will further increase the understanding on the influence of common power device processes steps on SiC defect characteristics, with the main focus on the aforementioned three processes, epitaxial layer growth, ion implantation and high temperature surface treatments. Simultaneous independent process development and improvement for each respective process step will take place.
The next steps considering defect characterization cover different investigation ranging from the influence of different SiC substrate wafer suppliers and cleaning procedures to the influence of different process steps on defect measurements. Consequently UV-PL measurements on patterned wafer and a correlation of measured surface and intrinsic defects with electric characteristics of processed chips are planned for the future.

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References

[1] J. Fan and P. K. Chu, *General Properties of Bulk SiC*, pp. 7–114. Cham: Springer International Publishing, 2014.
[2] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Japanese Journal of Applied Physics*, vol. 54, no. 4, pp. 40–103, 2015.
[3] N. Kaminski and O. Hilt, "SiC and GaN devices - wide bandgap is not all the same," *IET Circuits, Devices & Systems*, vol. 8, pp. 227–236(9), May. 2014.
[4] I. Chakarov and M. Temkin, "Modelling of ion implantation in SiC crystals," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 242, no. 1, pp. 690 – 692, 2006.
[5] Y. Sun, G. Feng, J. Zhang, W. Qian, and J. Kang, "Reduction of epitaxial defects on 4°-off 4H-SiC homo-epitaxial growth by optimizing in-situ etching process," *Superlattices and Microstructures*, vol. 99, pp. 145 – 150, 2016.
[6] C. Hecht, R. A. Stein, B. Thomas, L. Wehrhahn-Kilian, J. Rosberg, H. Kitahata, and F. Wischmeyer, "High-Performance Multi-Wafer SiC Epitaxy - First Results of Using a 10x100mm Reactor," in *Silicon Carbide and Related Materials 2009*, ser. Materials Science Forum, vol. 645, pp. 89–94, 2010.
[7] W. L. Lu, J. Li, Y. L. Fang, J. Y. Yin, and Z. H. Feng, "Triangular Defects Reduction and Uniformity Improvement of 4H-SiC Epitaxial Growth in a Planetary Reactor," in *Silicon Carbide and Related Materials 2017*, ser. Materials Science Forum, vol. 924, pp. 104–107, 2018.
[8] A. Henry, S. Leone, F. C. Beyer, H. Pedersen, O. Kordina, S. Andersson, and E. Janzen, "SiC epitaxy growth using chloride-based CVD," *Physica B: Condensed Matter*, vol. 407, no. 10, pp. 1467 – 1471, 2012.
[9] T. Kimoto, "Bulk and epitaxial growth of silicon carbide," *Progress in Crystal Growth and Characterization of Materials*, vol. 62, no. 2, pp. 329 – 351, 2016.
[10] W. Daves, A. Krauss, V. Häublein, A. J. Bauer, and L. Frey, "Enhancement of the Stability of Ti and Ni Ohmic Contacts to 4H-SiC with a Stable Protective Coating for Harsh Environment Applications," *Journal of Electronic Materials*, vol. 40, no. 9, p. 1990, Jun. 2011.
[11] D. Cho, K. Park, S. Yoo, S. Kim, J. Lee, and K. Kim, "A study on N_2O direct oxidation process with re-oxidation annealing for the improvement of interface properties in 4H-SiC MOS capacitor," *Journal of the Korean Physical Society*, vol. 71, no. 3, pp. 150–155, Aug. 2017.
[12] N. Preissler, C. T. Trinh, M. Trahms, P. Sonntag, D. Abou-Ras, H. Kirmse, R. Schlatmann, B. Rech, and D. Amkreutz, "Impact of Dielectric Layers on Liquid-Phase Crystallized Silicon Solar Cells," *IEEE Journal of Photovoltaics*, vol. 8, no. 1, pp. 30–37, Jan. 2018.
[13] Z. Wang, W. Liu, and C. Wang, "Recent Progress in Ohmic Contacts to Silicon Carbide for High-Temperature Applications," *Journal of Electronic Materials*, vol. 45, no. 1, pp. 267–284, Jan. 2016.
[14] M. V. Rao, "Maturing ion-implantation technology and its device applications in SiC," *Solid-State Electronics*, vol. 47, no. 2, pp. 213 – 222, 2003.
[15] A. Hallen and M. Linnarsson, "Ion implantation technology for silicon carbide," *Surface and Coatings Technology*, vol. 306, pp. 190 – 193, 2016.
[16] R. Nipoti, H. M. Ayedh, and B. G. Svensson, "Defects related to electrical doping of 4H-SiC by ion implantation," *Materials Science in Semiconductor Processing*, vol. 78, pp. 13 – 21, 2018.
[17] J. Cheng and B. Tsui, "Effects of Rapid Thermal Annealing on Ar Inductively Coupled Plasma-Treated n-Type 4H-SiC Schottky and Ohmic Contacts," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3739–3745, Sep. 2018.
[18] E. van Brunt, A. Burk, D. J. Lichtenwalner, R. Leonard, S. Sabri, D. A. Gajewski, A. Mackenzie, B. Hull, S. Allen, and J. W. Palmour, "Performance and Reliability Impacts of Extended Epitaxial Defects on 4H-SiC Power Devices," in *Silicon Carbide and Related Materials 2017*, ser. Materials Science Forum, vol. 924, pp. 137–142, 2018.
[19] N. Thierry-Jebali, C. Kawahara, T. Miyazawa, H. Tsuchida, and T. Kimoto, "Identification of Stacking Faults by UV Photoluminescence Imaging Spectroscopy on Thick, Lightly-Doped n-Type 4°-off 4H-SiC Epilayers," in *Silicon Carbide and Related Materials 2014*, ser. Materials Science Forum, vol. 821, pp. 323–326, 2015.