Chip/Package/Board/System Co-Design

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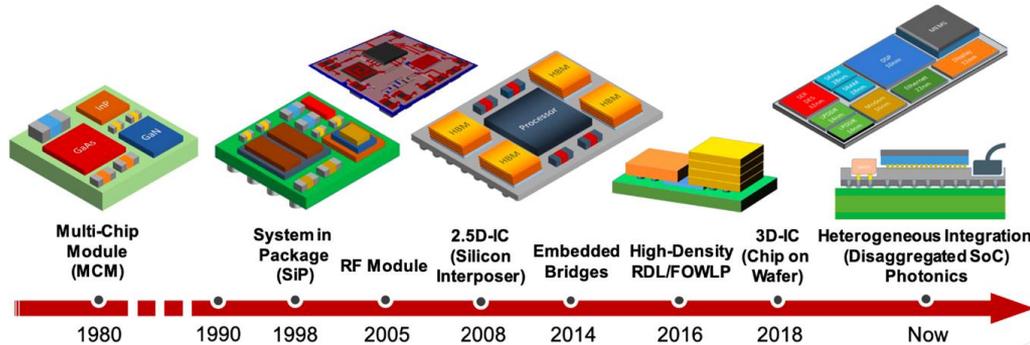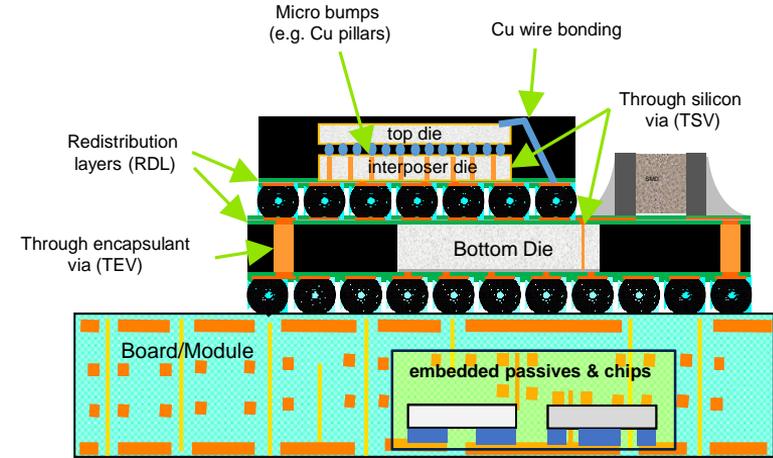# Outline

1. Design methodology for heterogeneous integration

2. Parts of a generic chip/package/board/system co-design flow

3. The need for a "multi-dimensional" modular design environment

4. File based design environment – standardized file formats

5. Coherent layout design environment for chip+package+board

6. Assembly design kits (ADKs)

7. 3D model generation (link to 3D EM field simulation)

8. Inter-company data exchange

9. Conclusion & outlook

Outline

A Heterogeneous World

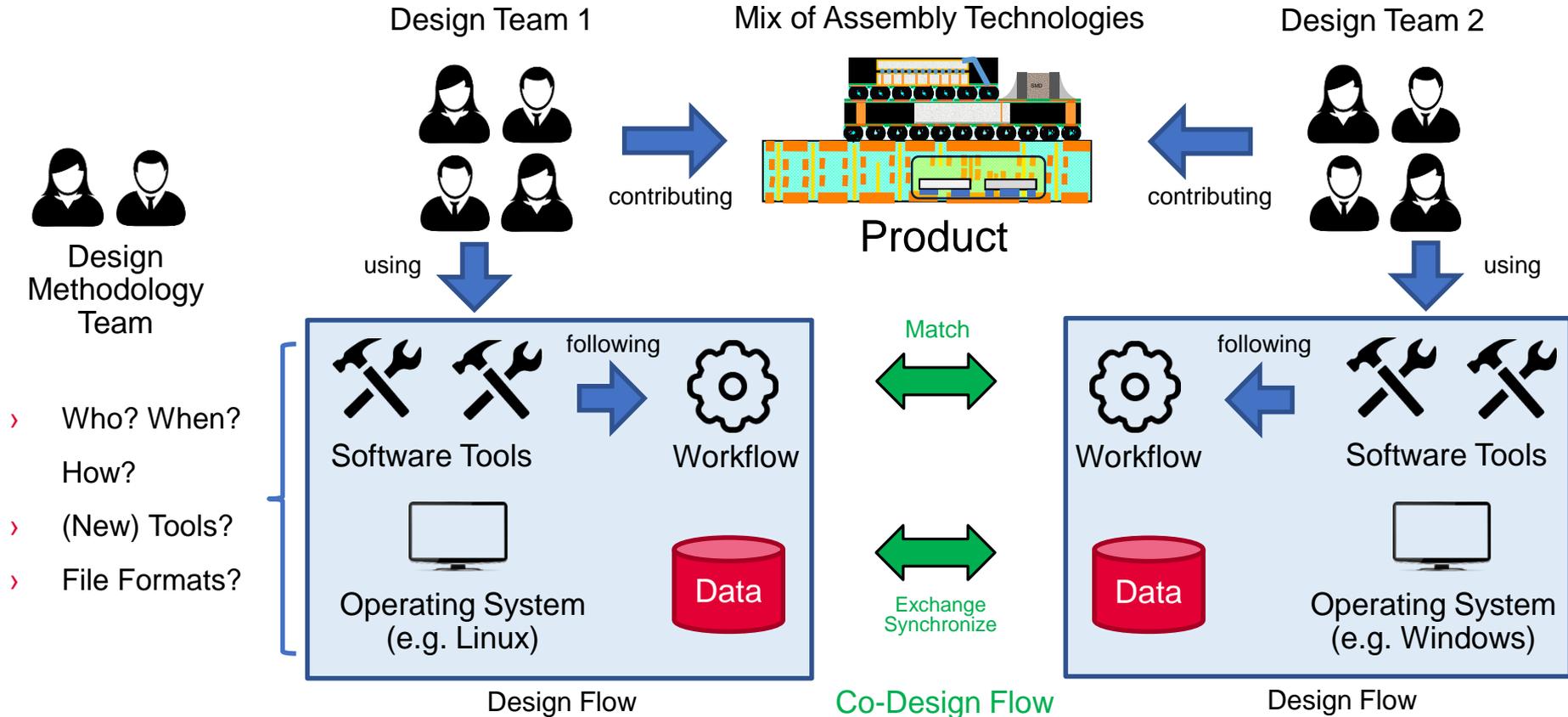› Products with integrated circuits are getting more and more heterogeneous …

Source: Semiconductor-Engineering, Cadence

› Engineers need to be supported by software → „Design Automation"
  – Mechanical Computer-Aided-Design (CAD) → full-blown 3D design
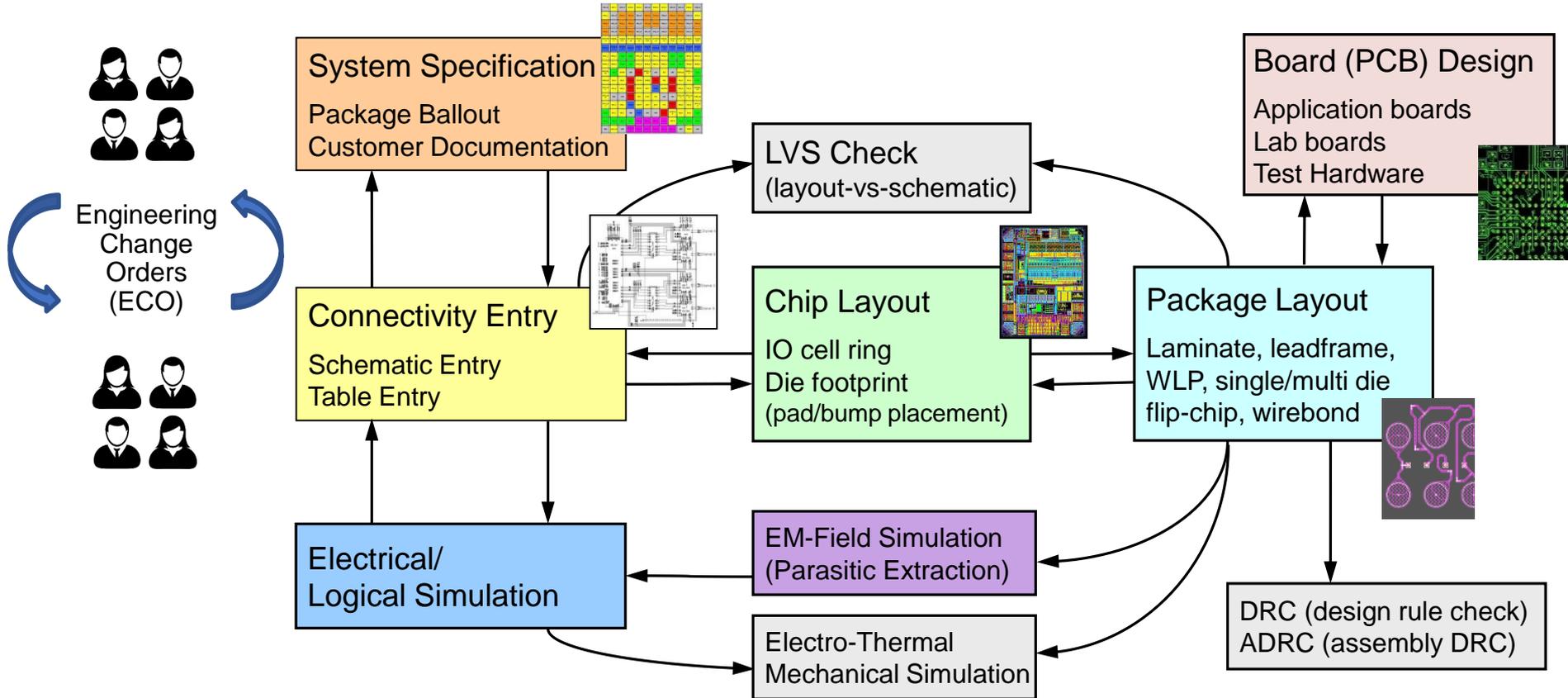 – Electrical CAD („Electronic Design Automation") → usually 2,5D design

What is Design Methodology?

Outline

Chip/Package/Board Co-Design Flow

Engineering Change Orders (ECO)

System Specification

Package Ballout
Customer Documentation

Connectivity Entry

Schematic Entry
Table Entry

Electrical/ Logical Simulation

LVS Check
(layout-vs-schematic)

Chip Layout

IO cell ring
Die footprint
(pad/bump placement)

EM-Field Simulation
(Parasitic Extraction)

Electro-Thermal Mechanical Simulation

Package Layout

Laminate, leadframe, WLP, single/multi die flip-chip, wirebond

Board (PCB) Design

Application boards
Lab boards
Test Hardware

DRC (design rule check)
ADRC (assembly DRC)

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Modularization
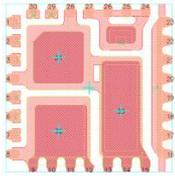
› Design of Heterogeneous Integration Products requires …

… a Modular Design Environment

› Modularization in
Assembly Technology

FO-WLP   Leadframe   Laminates

› Modularization in Design Tools
› Modularization in Configuration
(Assembly Design Kits – ADKs)
› Modularization in Data Exchange
(standardized file formats)
› Modularization in Design Environments
– Windows vs Linux
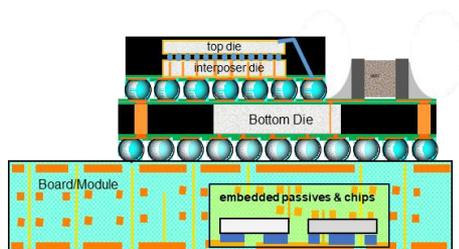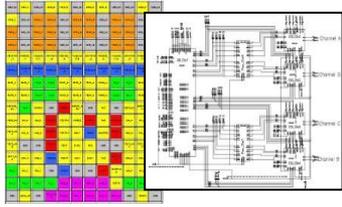– Inter-company data exchange
› Modularization in Work Flows

Outline

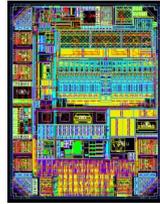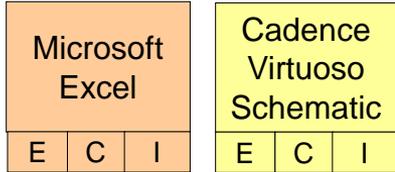IPCEI
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File Based Co-Design
(Modularization in Design Environments, Tools & Data Exchange)

System Development   Chip Development   Package Development   Board Development

Ballout & System Spec   Chip Layout   Laminate   FO-WLP   Leadframe   PCB
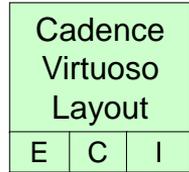
Microsoft Excel	Cadence Virtuoso Schematic	Cadence Virtuoso Layout	Cadence Virtuoso CDNSIP	Cadence Virtuoso Layout	Autodesk AutoCAD	Cadence Allegro PCB
E C I	E C I	E C I	E C I	E C I	E C I	E C I

Export
Compare
Import

Package Connectivity

Die Footprint

Package Layout

PCB Layout

Design Project 1

Data Repo (UNIX) — File Sync — Data Repo (UNIX) — Design Project 2 — Data Repo (Windows) — Internet — Data Repo (other Company)

GIT, Microsoft Sharepoint, …   Inter-Company Data Exchange

Design Project and Configuration
(Modularization in Configuration)

› Project configuration
  – Process Design Kit (PDK)
  – One or more Assembly Design Kits (ADK)

› Traceability by
  – Read-only project configuration
  – Design flow version
  – PDK + ADK versions

Unix Fileserver Read-only

Chip PDK

Package ADK

Data Management (DM) Repository

No-DM Unix-Fileserver

Project Configuration

data access

User "enters" design project

Tool Wrapper
Create/set environment

EDA Tool

part of

Files in Working-Dir

Wrappers Scripts Tool Extensions

Infineon Design Flow v?.?

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Die Footprint Extraction

› Several (quasi) standards exist:
  – Cadence XML-Die-Abstract (XDA)
  – LSI-Package-Board (LPB) - IEEE-2401
  – Artwork AIF
    – Easily readable and extendable
    – Supported by some 3rd party tools as well (at least the "core data")

```
[DIE]
NAME=example_die
WIDTH=1900.00
HEIGHT=2600.00

[PADS]
die_pad1=RECT 70.00 70.00

[NETLIST]
VSS:G   1   die_pad1   -600.00   -1200.00
CLK:I   2   die_pad1   -472.00   -1200.00
A<0>:B  3   die_pad1   -300.00   -1200.00

[IFX_DATA]
CREATION_DATE=Feb 28 19:12:07 2009
USER=unixuser
DIE_TYPE=IC
…

[IFX_LAYER]
DESCRIPTION=top metal layer
RECT -600,-600 500,500
…
```
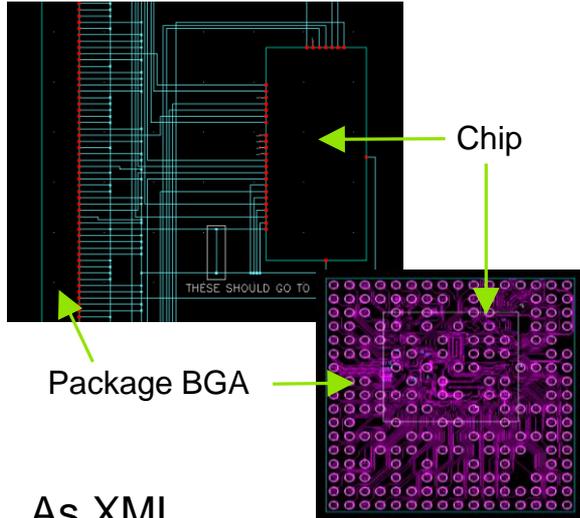
Basic data about die

Shape of die pads

Position of die pads
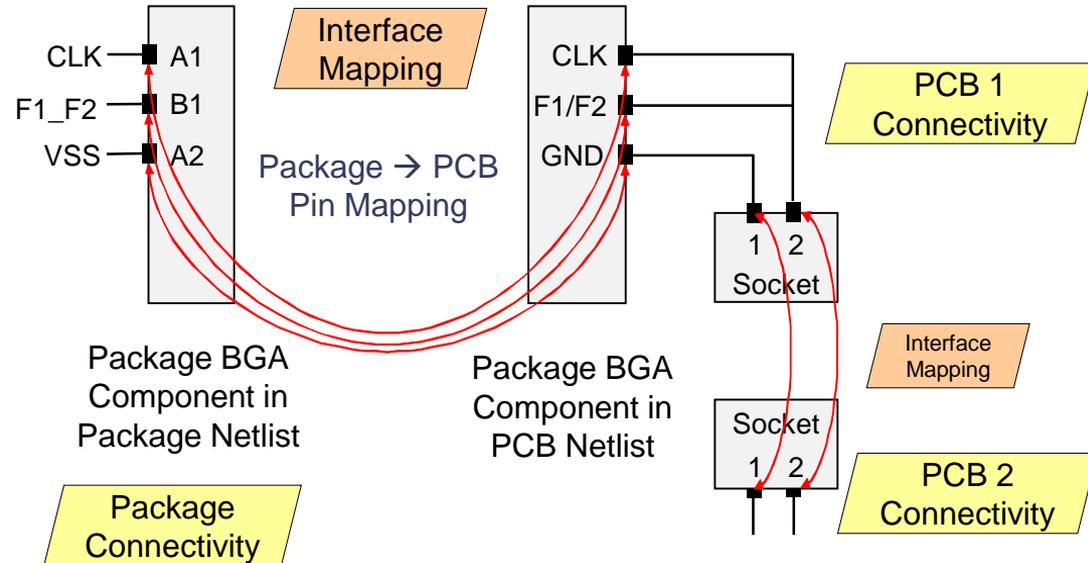
Additional meta data

Additional design layer

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File Formats (2): System Netlist
(Modularization in Tools & Data Exchange)

› ## Package Connectivity
  – ### As Schematic

Chip

Package BGA

  – ### As XML

```
<net id="VSS">
  <connects>
    <connect cellInstanceRef="BGA" portRef="A2"/>
    <connect cellInstanceRef="DIE" portRef="3"/>
```

› ## Hierarchical System Connectivity

Interface Mapping

PCB 1 Connectivity

Package → PCB Pin Mapping

CLK
F1_F2
VSS
A1
B1
A2

CLK
F1/F2
GND

1 2
Socket

Socket
1 2

Interface Mapping

PCB 2 Connectivity

Package BGA Component in Package Netlist

Package BGA Component in PCB Netlist

Package Connectivity

› Independent design files
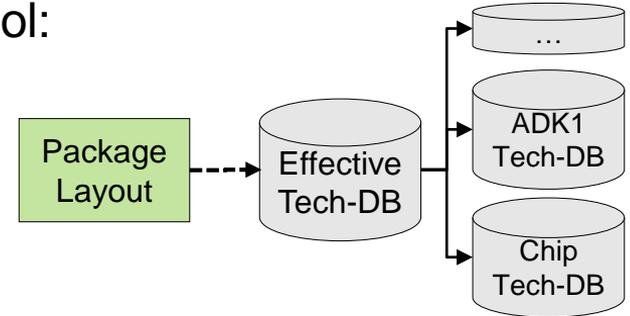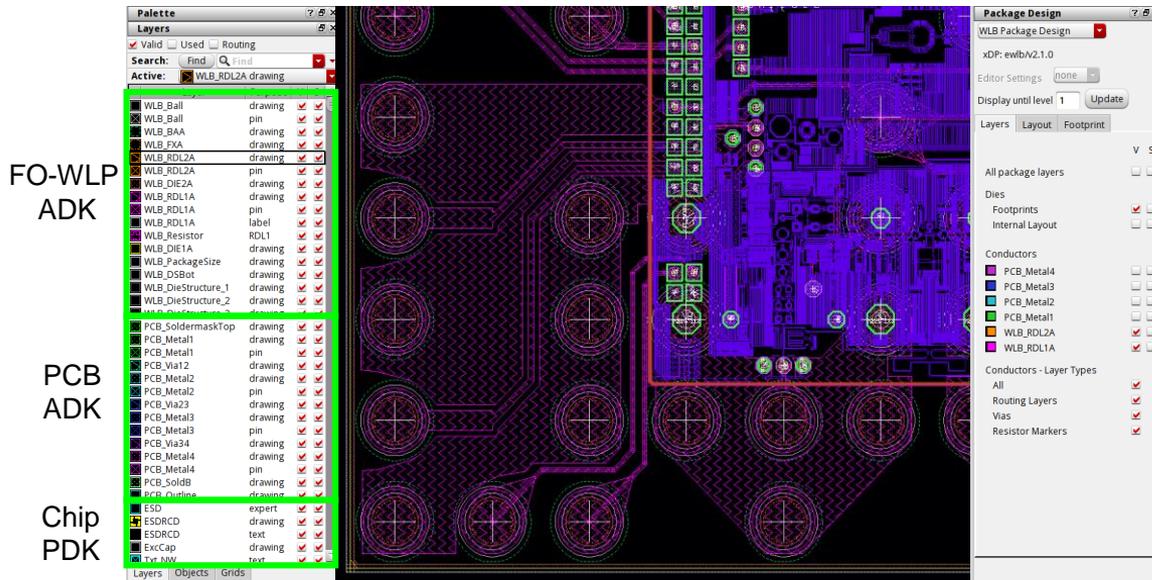› Can be handled independently by different design teams even in different companies!

Outline

Coherent Layout Design Environment (1)
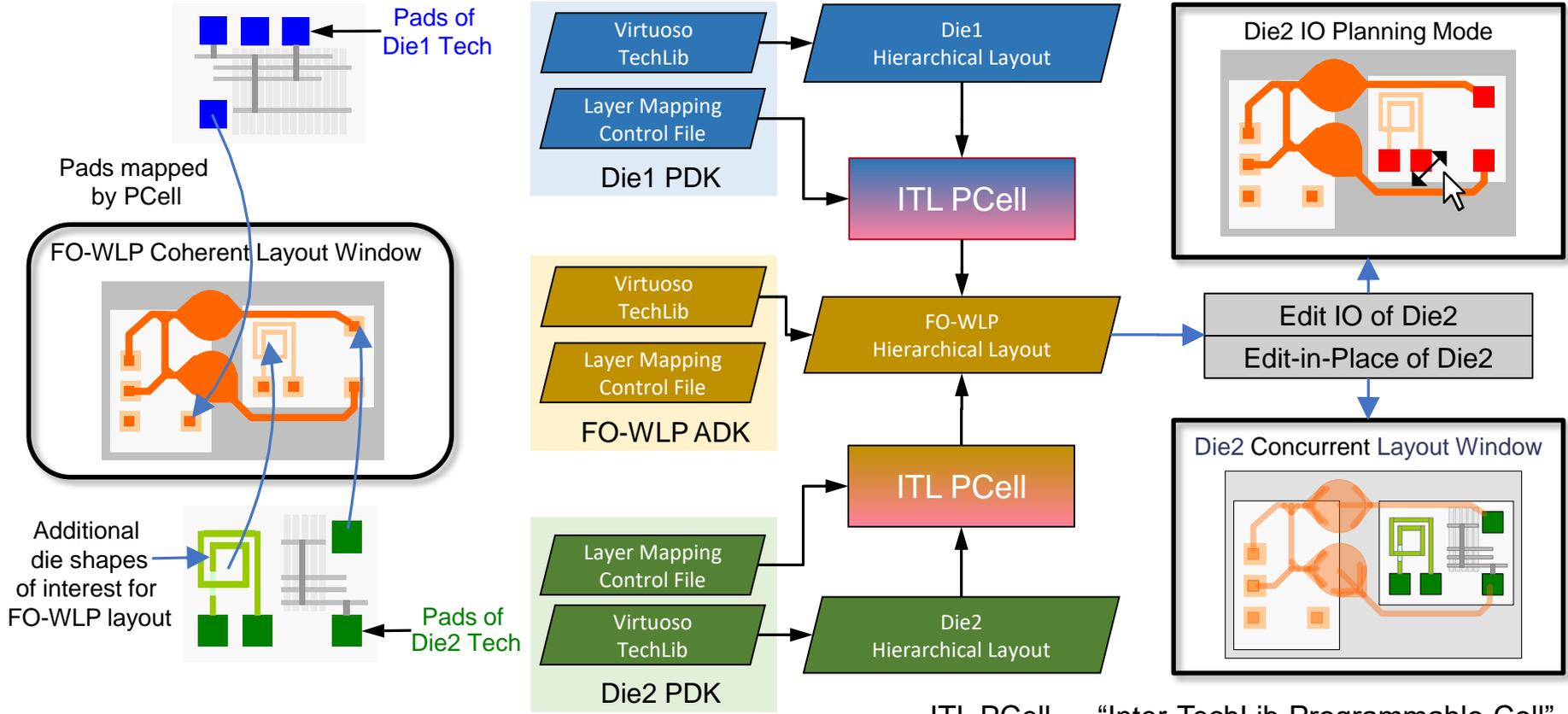(Modularization in Technology)

› Traditionally chip, package, and board layout is done in separate software tools
› Chip + FO-WLP + Board layout design in one EDA tool:

› OpenAccess Technology Database (Cadence Virtuoso)

› Feature: "Incremental Tech-DB"
› Originally used to define different chip technology options
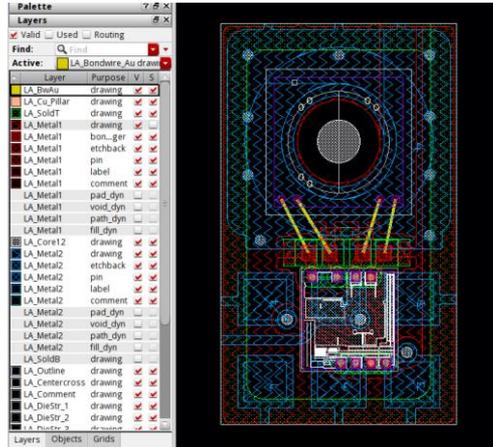› We exploit that feature for "multi-technology" layout design

Coherent Layout Design Environment (2)
(Modularization in Technology)

Pads of Die1 Tech

Pads mapped by PCell

FO-WLP Coherent Layout Window

Additional die shapes of interest for FO-WLP layout

Pads of Die2 Tech

Virtuoso TechLib

Die1 Hierarchical Layout

Layer Mapping Control File

Die1 PDK

ITL PCell

Die2 IO Planning Mode

Virtuoso TechLib

FO-WLP Hierarchical Layout

Layer Mapping Control File

FO-WLP ADK

Edit IO of Die2

Edit-in-Place of Die2

ITL PCell

Die2 Concurrent Layout Window

Layer Mapping Control File

Die2 Hierarchical Layout

Virtuoso TechLib

Die2 PDK

ITL PCell … "Inter-TechLib Programmable Cell"

Coherent Layout Design Environment (3)
(Modularization in Technology)

› Laminate Package Design
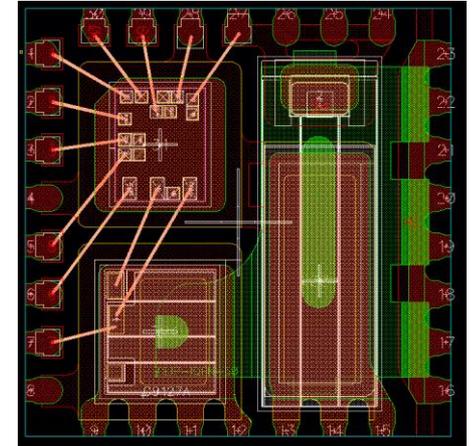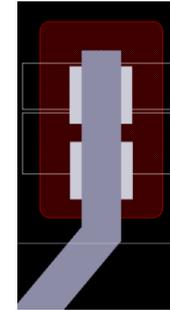

› Bondwires
› Cu-Pillars

› BGA Editor
› Padstack Editor

Support for curvilinear layout shapes

› Leadframe Package Design

› Clips
› Soldered Flip-Chip
› Double-Stitch Bondwires
› Bond ribbons
› …

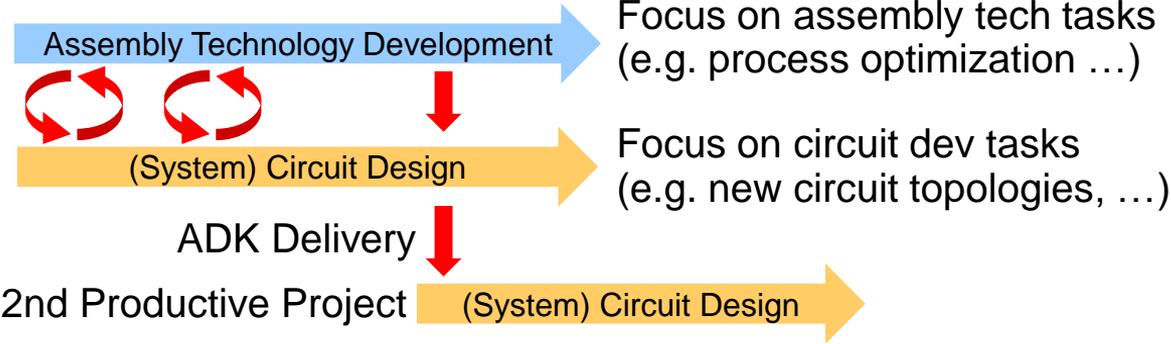MIKON 2020

Outline

Assembly Design Kits
(Modularization in Work Flow, Tools & Configuration)

Lead/Pilot Project

Assembly Technology Development → Focus on assembly tech tasks (e.g. process optimization …)

(System) Circuit Design → Focus on circuit dev tasks (e.g. new circuit topologies, …)

ADK Delivery

2nd Productive Project — (System) Circuit Design

Config Files about
› Layer Data
› Layer Mapping Data
› Materials
› Bondwire & Options
› …

ADK Content Directory

XML → Config File for Tool A → Valid for Tool version 1.0 → Valid for Tech Option X → File 1

Config File for Tool B → Valid for Tool version 2.0 → Valid for Tech Option Y → File 2

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Modular 3D-Model-Generation
(Modularization in Technology & Tools)

Chip + Package Model in 3D
With Material Assignment

Ready for EM Field Simulation …

Chip PDK
- Connectivity through chip layers
- Shape simplification rules per layer
- Chip layer stack (material, thickness)

Package ADK
- Connectivity through package layers
- Shape simplification rules per layer
- Package layer stack (material, thickness)

Chip + Package Layout (2,5D)

- Net Extraction
- Layout Simplification
- Layout Export

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Inter-Company Data Exchange
(Modularization in Design Environment)

Company B
(Chip Integrator)

PCB Design

Component Library

Layout Footprint

Schematic Symbol

Translation to PCB tool specific format

Internet

Layout Footprint Schematic Symbol

Gateway

GIT, MS Sharepoint

Company A
(Chip Manufacturer)

Excel Sheet

Package Interface (XML)

Design Concept: Definition of Package Ballout

Consistency checks

Ballout Data

Data Filtering

Design Project

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Conclusion and Outlook

› At Infineon most of new package designs are already done with this common chip/package/board co-design flow – used by > 50 engineers
  – Design flow for heterogeneous integration also highly beneficial for "standard" systems

› Versatile heterogeneous layout environment – linked with versatile ADK concept
  – ADKs for different lead frame package families (QFP, SO, TO, …)
  – ADK for LGA & BGA
  – ADK for FO-WLP

› Next steps:
  – Introduce even more modular approach for ADKs ("ADK-lets")
  – Introduce tighter link between 2,5D E-CAD and 3D M-CAD

Lead frame

Interposer 1

Bond wires

Interposer 2
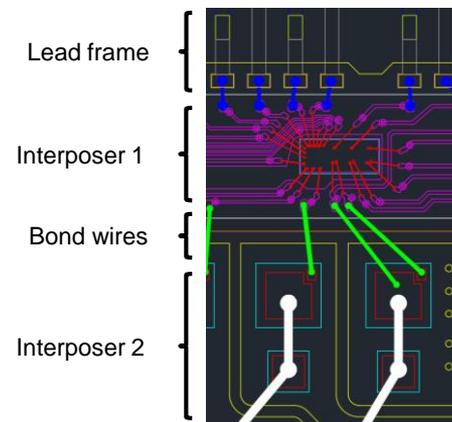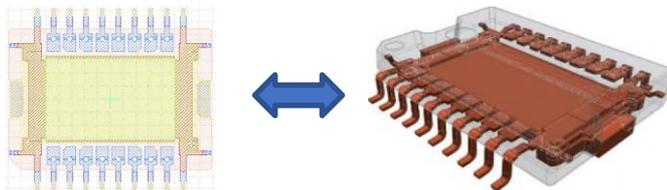
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