Chip/Package/Board/System Co-Design

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Outline

1. Design methodology for heterogeneous integration
2. Parts of a generic chip/package/board/system co-design flow
3. The need for a “multi-dimensional” modular design environment
4. File based design environment – standardized file formats
5. Coherent layout design environment for chip+package+board
6. Assembly design kits (ADKs)
7. 3D model generation (link to 3D EM field simulation)
8. Inter-company data exchange
9. Conclusion & outlook

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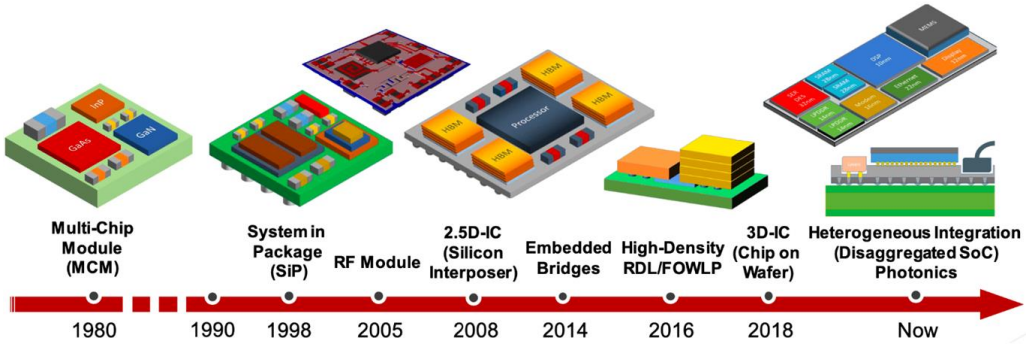
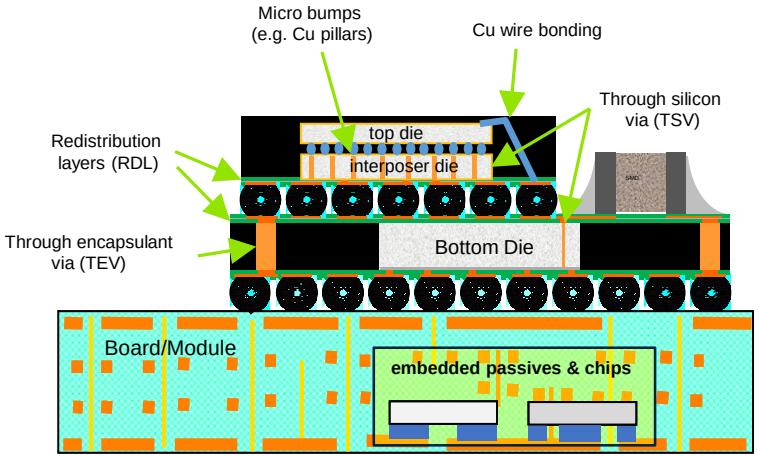
A Heterogeneous World

› Products with integrated circuits are getting more and more heterogeneous …

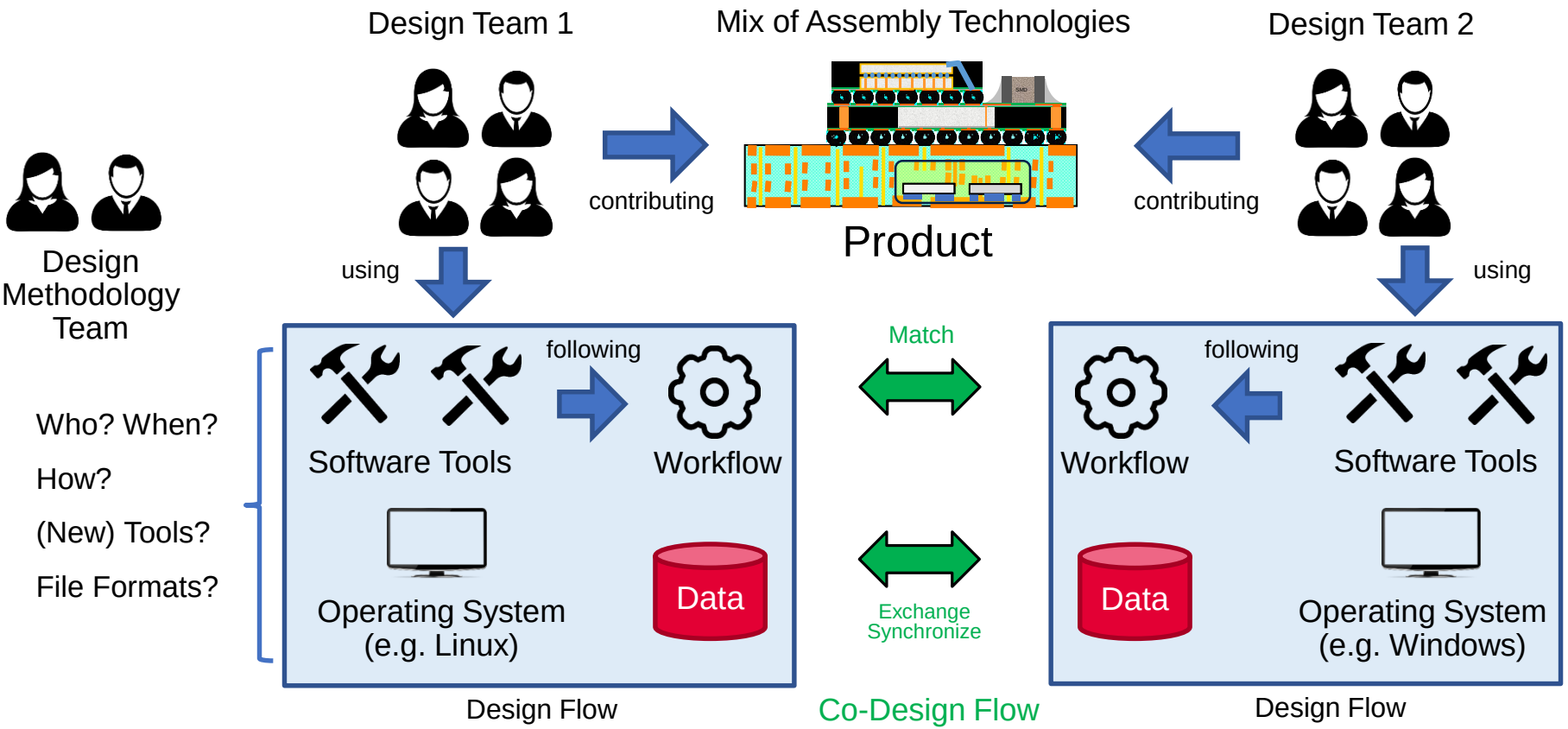


Source: Semiconductor-Engineering, Cadence



› Engineers need to be supported by software → „Design Automation“
- Mechanical Computer-Aided-Design (CAD) → full-blown 3D design
- Electrical CAD („Electronic Design Automation“) → usually 2,5D design

What is Design Methodology?



- Who? When?
  How?
- (New) Tools?
- File Formats?

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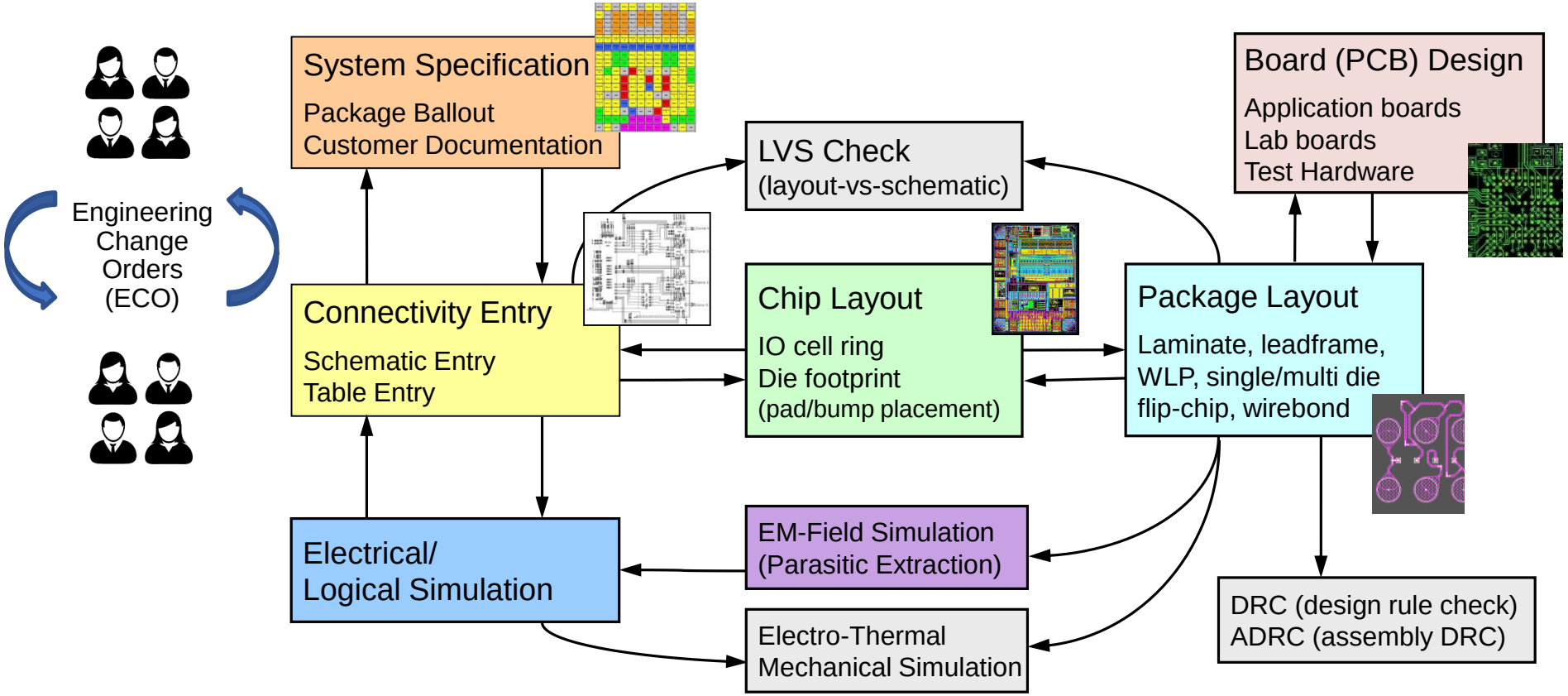
Chip/Package/Board Co-Design Flow



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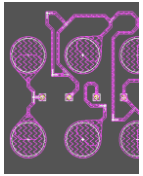
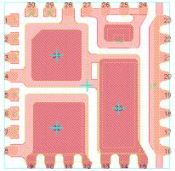
Modularization

- Design of Heterogeneous Integration Products requires …
  … a Modular Design Environment

- Modularization in Assembly Technology

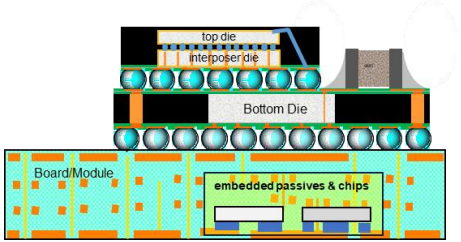


FO-WLP



Leadframe

Laminates



- Modularization in Design Tools
- Modularization in Configuration
  (Assembly Design Kits – ADKs)
- Modularization in Data Exchange
  (standardized file formats)
- Modularization in Design Environments
  - Windows vs Linux
  - Inter-company data exchange
- Modularization in Work Flows

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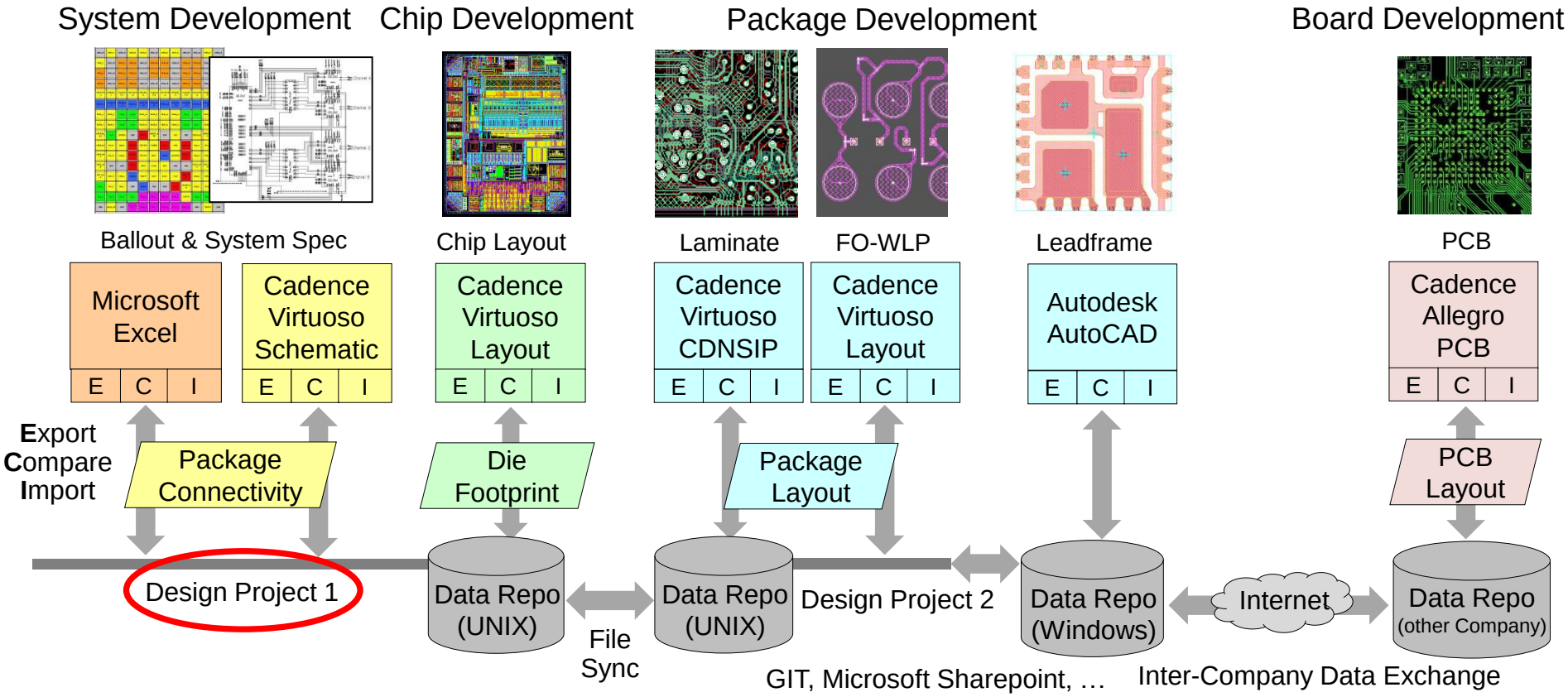
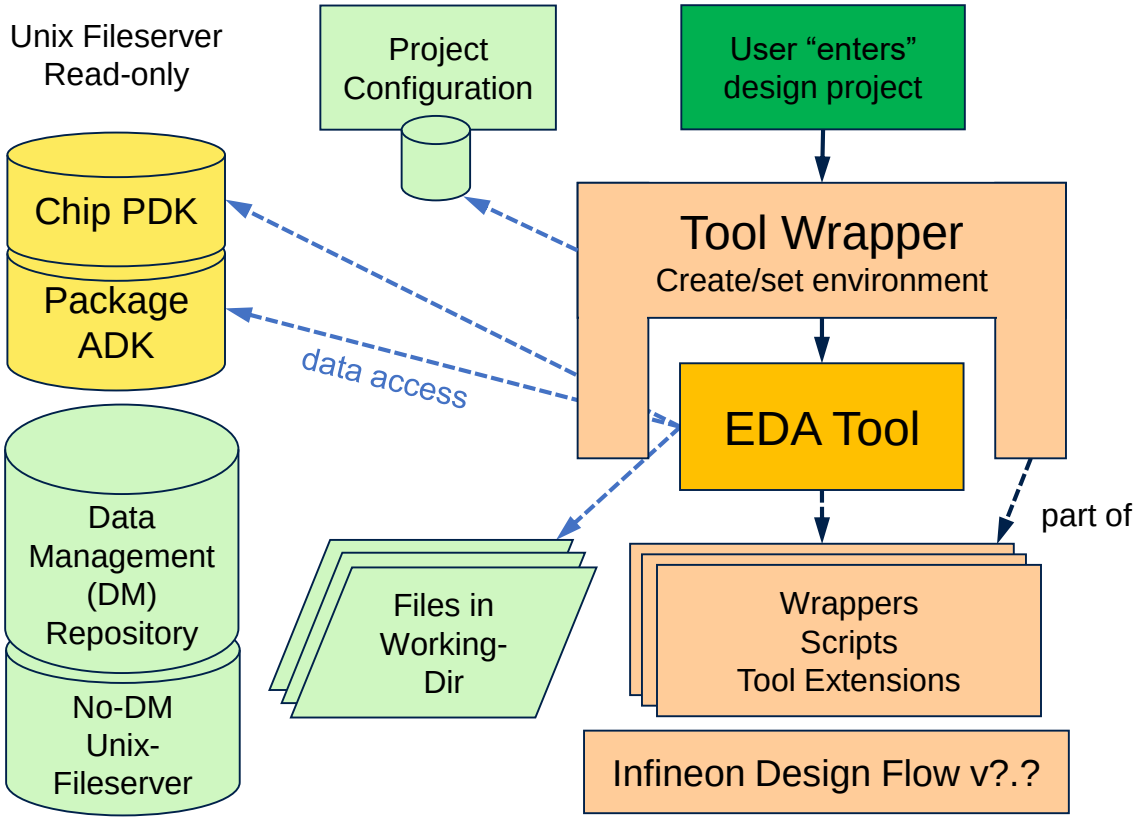
File Based Co-Design
(Modularization in Design Environments, Tools & Data Exchange)



Design Project and Configuration
(Modularization in Configuration)

- Project configuration
  - Process Design Kit (PDK)
  - One or more Assembly Design Kits (ADK)
- Traceability by
  - Read-only project configuration
  - Design flow version
  - PDK + ADK versions



File Formats (1): Die Footprint
(Modularization in Tools & Data Exchange)

Die Footprint Extraction

- Several (quasi) standards exist:
  - Cadence XML-Die-Abstract (XDA)
  - LSI-Package-Board (LPB) - IEEE-2401
  - Artwork AIF
    - Easily readable and extendable
    - Supported by some 3rd party tools as well (at least the “core data”)

```
[DIE]
NAME=example_die
WIDTH=1900.00
HEIGHT=2600.00

[PADS]
die_pad1=RECT 70.00 70.00

[NETLIST]
VSS:G  1  die_pad1  -600.00  -1200.00
CLK:I  2  die_pad1  -472.00  -1200.00
A<0>:B 3  die_pad1  -300.00  -1200.00

[IFX_DATA]
CREATION_DATE=Feb 28 19:12:07 2009
USER=unixuser
DIE_TYPE=IC
…

[IFX_LAYER]
DESCRIPTION=top metal layer
RECT -600,-600 500,500
…
```

Basic data about die

Shape of die pads

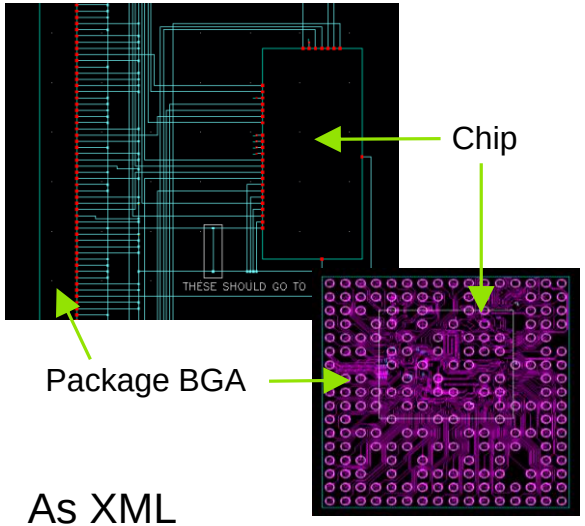
Position of die pads

Additional meta data

Additional design layer

File Formats (2): System Netlist
(Modularization in Tools & Data Exchange)

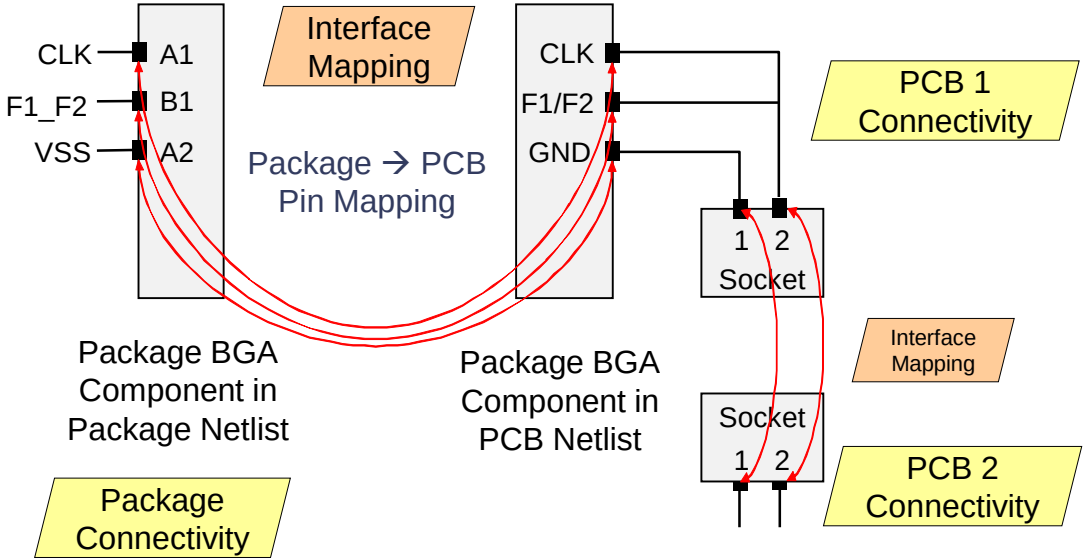
- Package Connectivity
  - As Schematic



  - As XML

```
<net id="VSS">
  <connects>
    <connect cellInstanceRef="BGA" portRef="A2"/>
    <connect cellInstanceRef="DIE" portRef="3"/>
```

- Hierarchical System Connectivity



- Independent design files
- Can be handled independently by different design teams even in different companies!

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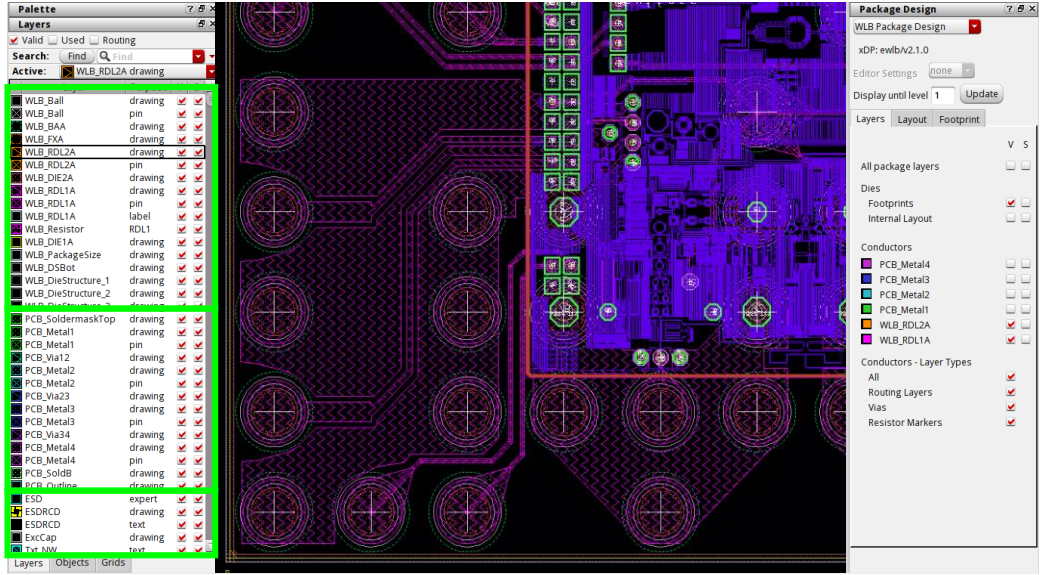
Coherent Layout Design Environment (1)
(Modularization in Technology)

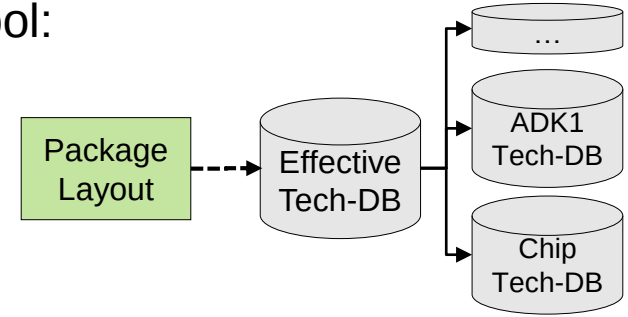
- Traditionally chip, package, and board layout is done in separate software tools
- Chip + FO-WLP + Board layout design in one EDA tool:

FO-WLP ADK

PCB ADK

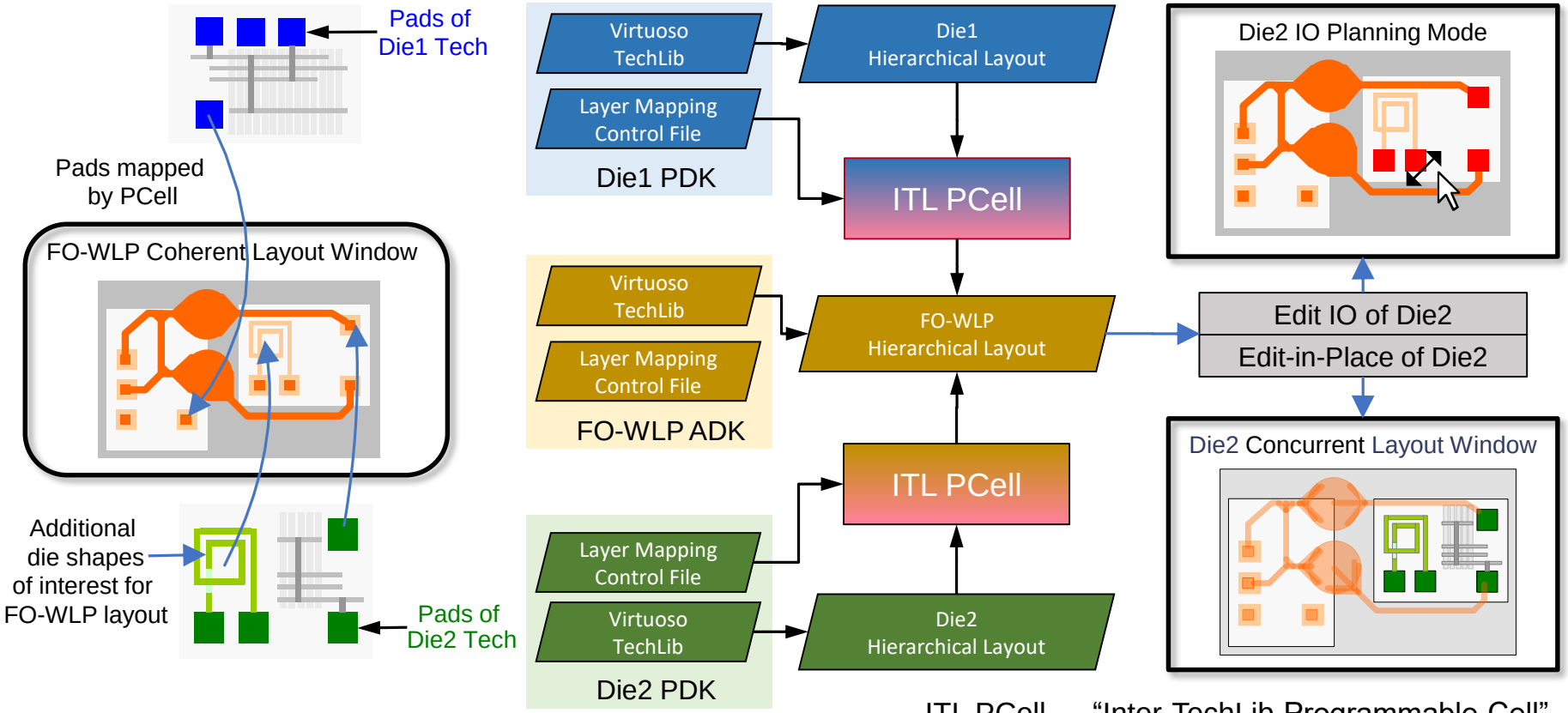
Chip PDK





- OpenAccess Technology Database (Cadence Virtuoso)
- Feature: “Incremental Tech-DB”
- Originally used to define different chip technology options
- We exploit that feature for “multi-technology” layout design

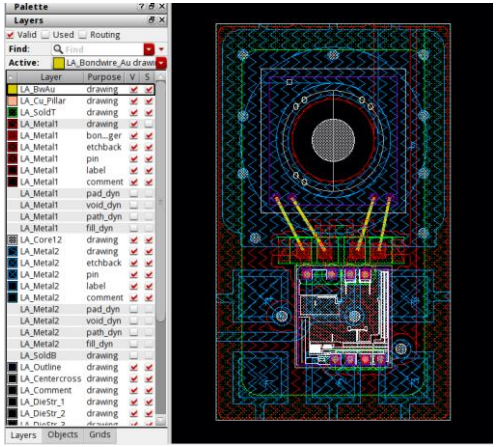
Coherent Layout Design Environment (2)
(Modularization in Technology)



ITL PCell … “Inter-TechLib Programmable Cell”

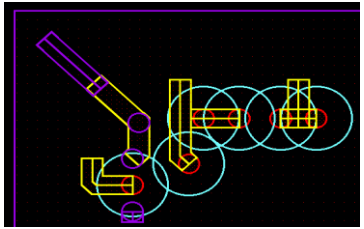
Coherent Layout Design Environment (3)
(Modularization in Technology)

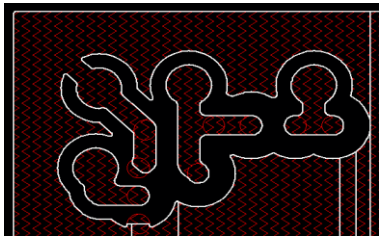
› Laminate Package Design



› Bondwires
› Cu-Pillars

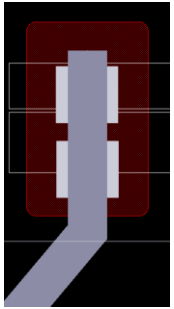
› BGA Editor
› Padstack Editor

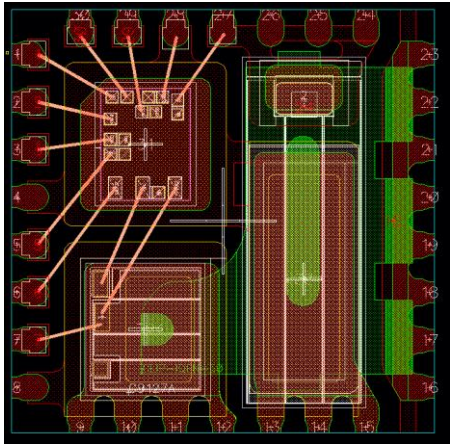




Support for curvilinear layout shapes

› Leadframe Package Design





› Clips
› Soldered Flip-Chip
› Double-Stitch Bondwires
› Bond ribbons
› …

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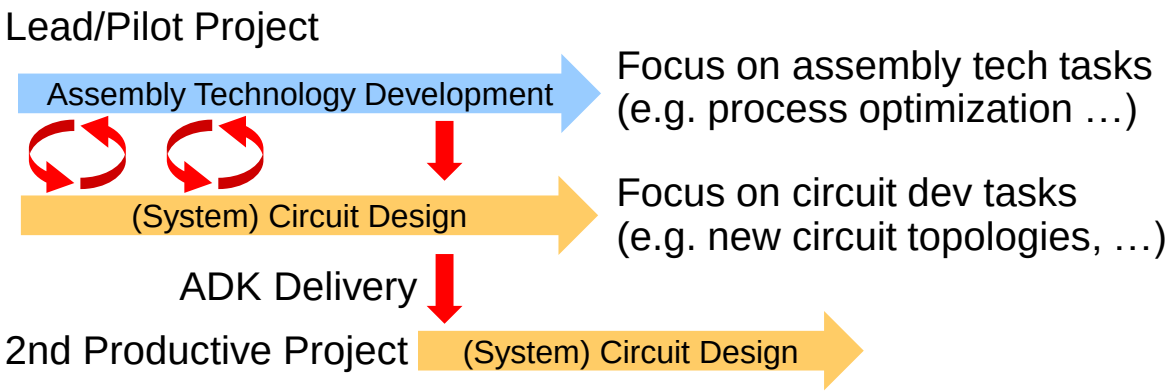
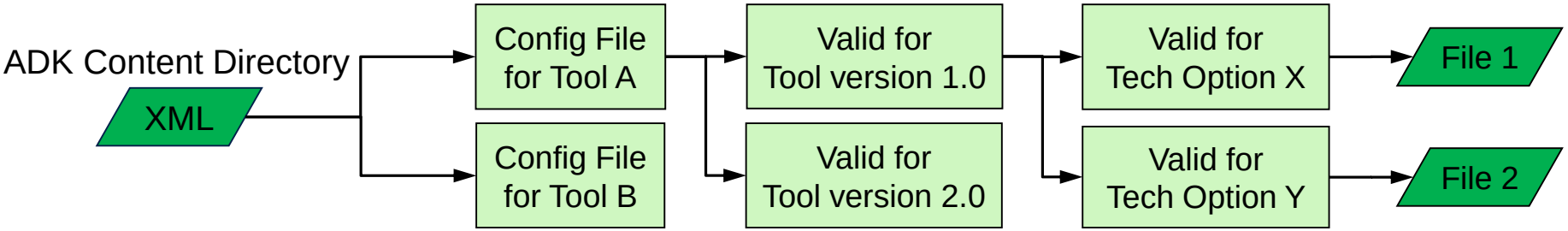
Assembly Design Kits
(Modularization in Work Flow, Tools & Configuration)



Config Files about

- Layer Data
- Layer Mapping Data
- Materials
- Bondwire & Options
- …



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Modular 3D-Model-Generation
(Modularization in Technology & Tools)

Connectivity through chip layers

Shape simplification rules per layer

Chip layer stack (material, thickness)

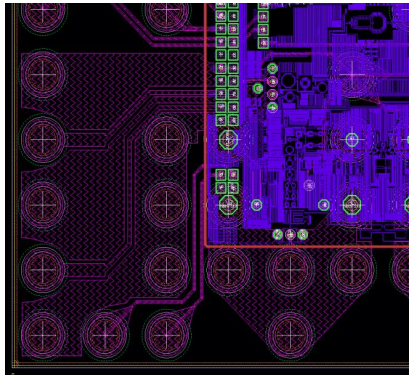
Chip PDK

Connectivity through package layers

Shape simplification rules per layer

Package layer stack (material, thickness)

Package ADK



Chip + Package Layout (2,5D)

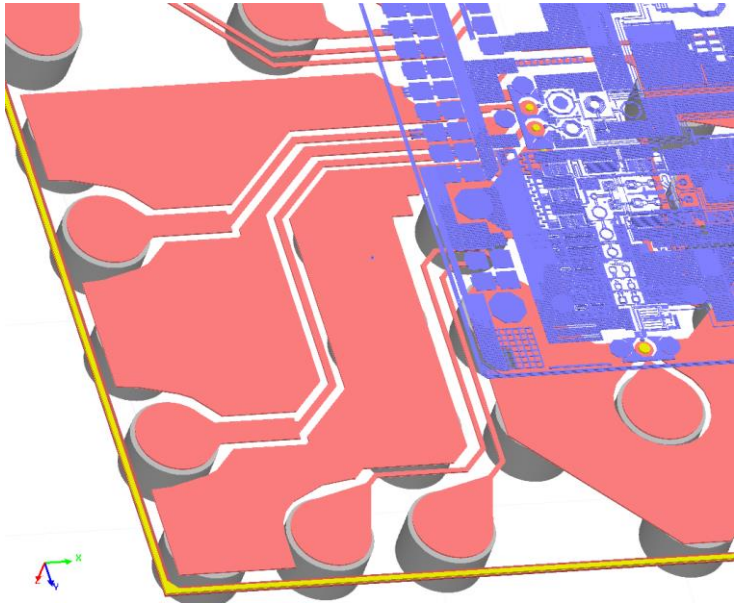
Net Extraction

Layout Simplification

Layout Export

Chip + Package Model in 3D
With Material Assignment

Ready for EM Field Simulation …



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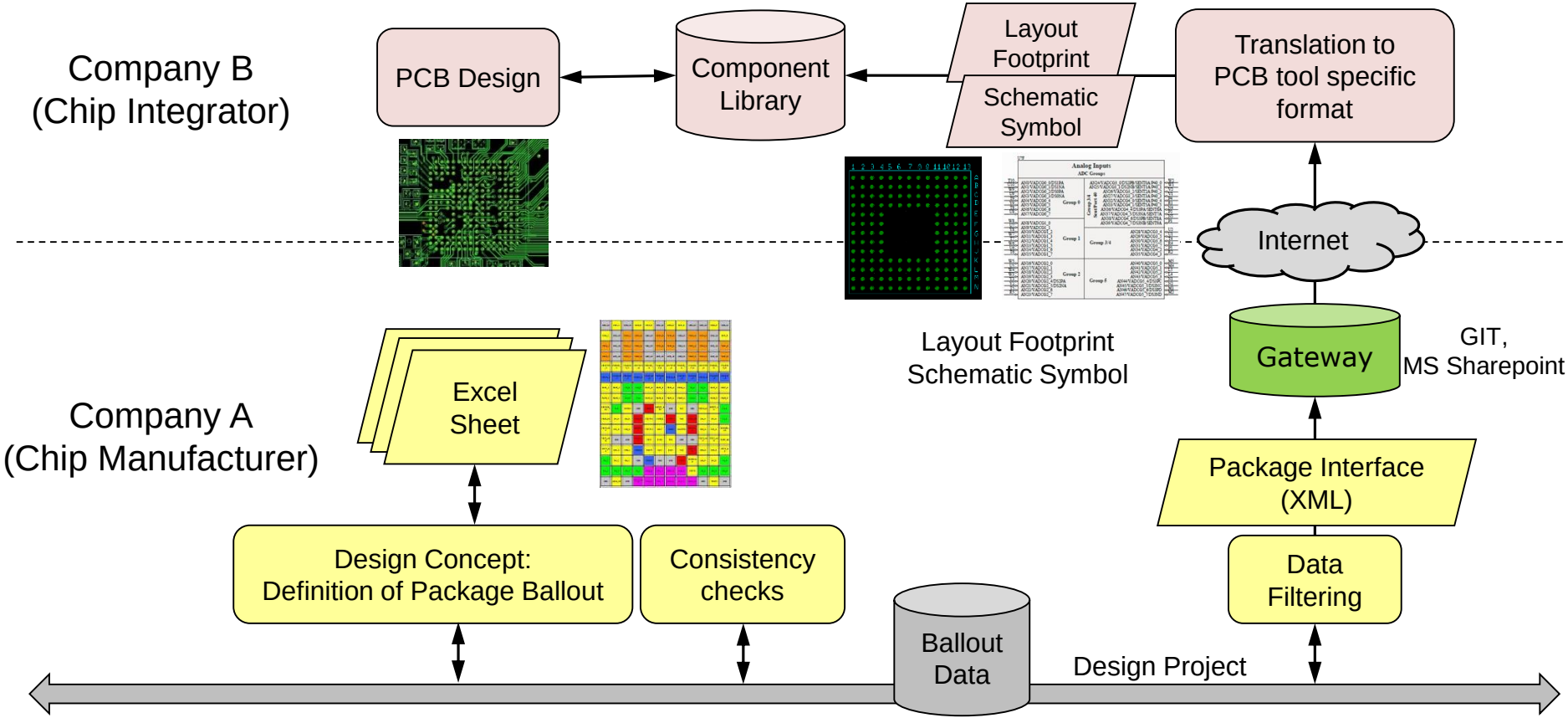
Inter-Company Data Exchange (Modularization in Design Environment)



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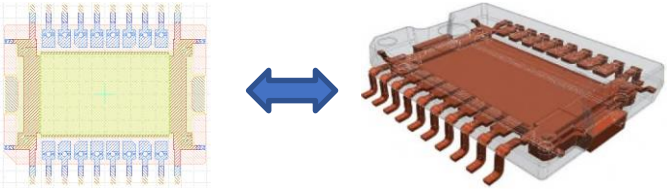
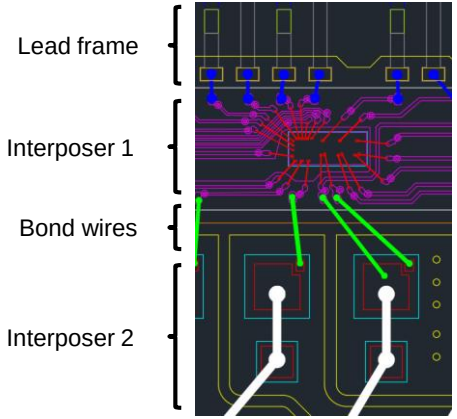
Conclusion and Outlook

- At Infineon most of new package designs are already done with this common chip/package/board co-design flow – used by > 50 engineers
  - Design flow for heterogeneous integration also highly beneficial for “standard” systems
- Versatile heterogeneous layout environment – linked with versatile ADK concept
  - ADKs for different lead frame package families (QFP, SO, TO, …)
  - ADK for LGA & BGA
  - ADK for FO-WLP
- Next steps:
  - Introduce even more modular approach for ADKs (“ADK-lets”)
  - Introduce tighter link between 2,5D E-CAD and 3D M-CAD





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