

Differential Reflective Metrology

An innovative variability measurement for advanced FDSOI material

J.-M. Billiez, W. Schwarzenbach
SOITEC

Parc Technologique des Fontaines, 38190 Bernin, France

Email of corresponding author: jean-michel.billiez@soitec.com, walter.schwarzenbach@soitec.com

Abstract

Thickness control is one of the key parameter to limit fully-depleted device variability. Differential Reflective Metrology (DRM) has been initially developed to measure SOI layer thickness variability at device scale. A 2nd generation DRM is proposed, both SOI & BOX layers thickness variability being now measured independently to each other, from device to wafer scale.

1. Fully Depleted SOI Layer and Device Variability

Beyond Smartphone era, the Internet of Thing, wearable electronics and automotive are big drivers for the growth of the semiconductor market. To achieve complex, miniaturized, ultra-low power and highly reliable circuits and to maintain sufficient performance and cost-effective solutions, planar Fully Depleted Silicon-On-Insulator (FD-SOI) on ultra-thin Buried Oxide (BOX) demonstrates benefits and capabilities through 28FD and 22FD technologies [1]. However, since Fully Depleted technology rely on undoped channel, Random Dopant Fluctuation does not contribute to V_T variability but channel silicon thickness (T_{Si}) itself appears as a new source of V_T variation, with an empirical correspondence close to 25mV/nm [2]. Accordingly, T_{Si} maximum fluctuation of 1nm has been considered as an initial objective for FD-SOI substrate development [3] and is delivered in manufacturing mode [4].

In order monitor properly T_{Si} fluctuation, SOI thickness variability across the full spatial frequency range has been considered, combining conventional ellipsometry for wafer-scale uniformity, atomic force microscopy (AFM) at sub-angstrom scale and the novel Differential Reflective Metrology (DRM) as described in [5]. DRM is used to monitor SOI layer thickness, then device variability at device scale.

Beyond already published early development and data, this paper intends to present updated results on DRM technology development, paving the way for a full wafer, device scale, SOI & BOX layer thickness variability measurement.

2. SmartCut Process for FD-SOI and 1st Gen DRM

The SmartCut process adapted to FD-SOI substrate preparation, as schematically shown on Figure 1, has already been published [4]. This process is based on wafer bonding of an implanted defect free donor substrate on a handle wafer, and requires extensive optimization including implant and thermal treatment process steps to transfer highly uniform, extremely thin SOI layers on ultra thin BOX. It considers a high temperature smoothing

option for wafer finishing, delivering ultra-low roughness SOI layers. Such surface roughness is associated to the SOI thickness variability at device scale.

Conventional dedicated DRM metrology is implemented in order to measure this SOI thickness variation at the device scale. 1st Gen DRM is based on the dependence of the optical reflectivity of a layer on its thickness. An appropriate wavelength / interferometry filter is chosen to maximize SOI layer dependence vs BOX variability contribution and built a 1D modeling, as shown on figure 2. For ultra-thin SOI and BOX layers, down to 4nm and 15nm respectively, as reported in [6], DRM measurement wavelength is thus determined *versus* SOI and BOX layers reflectivity in order to create a dedicated filter set for each product.

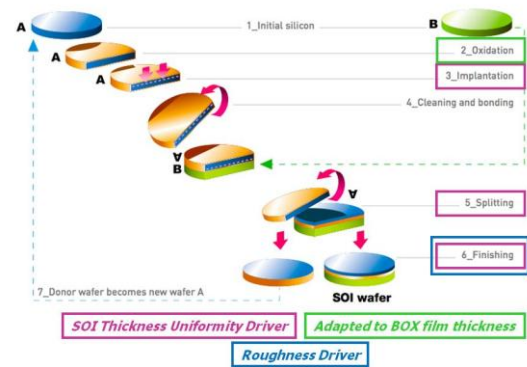


Figure 1: SmartCut Process Flow for FD-SOI Substrate Preparation

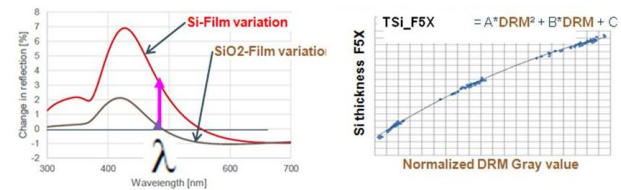


Figure 2 : 1st Gen DRM principle, associating single illumination wavelength choice (left) and 1D modeling (right)

3. 2nd Gen Differential Reflective Metrology

BOX variability influence on 1st Gen DRM measurement induces development needs to create a dual-wavelength 2nd Gen metrology. Figure 3 schematically shows principle of such generation, including (top) the simulated substrate reflectivity vs wavelength according to SOI & BOX thicknesses, considering this generation will support a dual camera, and (bottom) the corresponding 2D calibration vs SOI thickness, BOX thickness & DRM signal.

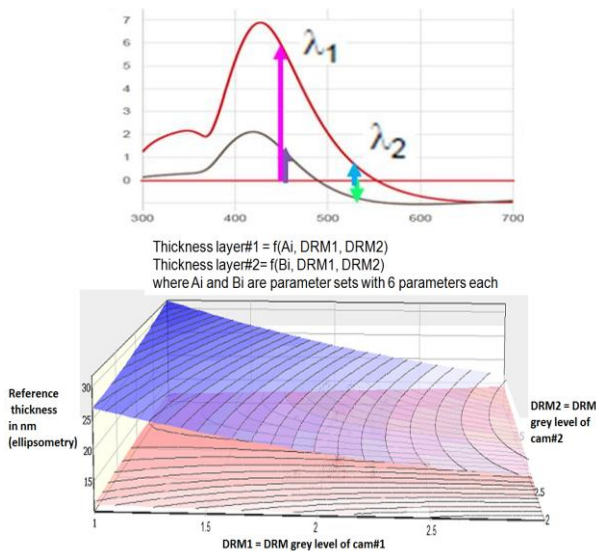


Figure 3: 1st Gen DRM principle, associating dual illumination wavelength choice (top) and 2D modeling (bottom)

Benefit of such 2D model is illustrated on Figure 4 which show thickness scale variability of both SOI (Fig 4a) & BOX (Fig 4b) layers at device scale.

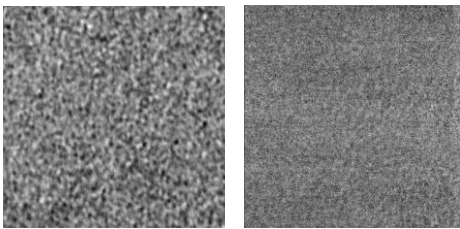


Figure 4: 22FDSOI product DRM measurement, (a) SOI layer (b) BOX layer, typical DRM 266x266 μm^2 scan image

Figure 5 highlight the benefit of a 2D modeling, allowing to remove the contribution of BOX variability in SOI layer thickness measurement. 2nd Gen can measure SOI variability independently to BOX thickness and also report BOX variability.

Hence, thanks to an adapted data acquisition & treatment protocole, including an appropriate optical hardware, we demonstrate ability of the 2nd Gen DRM to measure device scale thickness variability at the wafer scale [7]. Figure 6 shows high resolution thickness maps of SOI & BOX layers, measured on conventional 22FDSOI production wafers.

4. Conclusions

DRM dual-wavelength metrology is the response to the control of SOI variability of advanced FDSOI. The appropriate selection of wavelength and 2D calibration process gives flexibility to measure both ultra-thin SOI and BOX layers, down to 4nm and 15nm respectively.

The continuous acquisition mode gives extended thickness information from device scale to wafer scale.

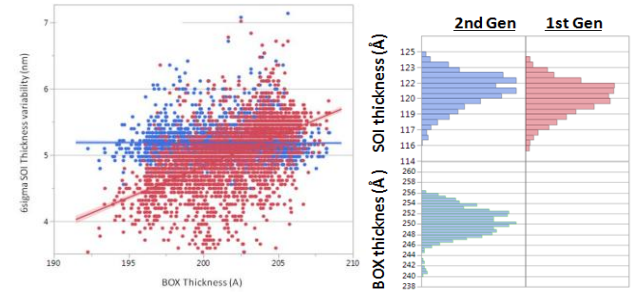


Figure 5: (Top) SOI vs BOX thickness variability as measured with a 1st Gen (red dots) and a 2nd Gen (blue dots) DRM tool. (Bottom) SOI and BOX thickness variation vs DRM metrology

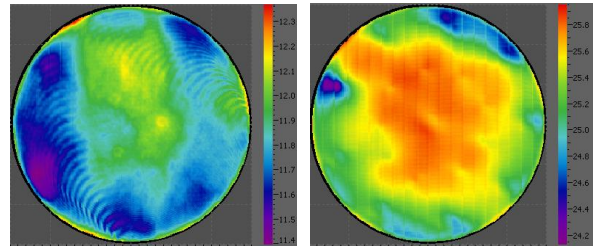


Figure 6: SOI (left) and BOX (right) layer thickness variation at device scale on a 300mm 22FDSOI wafer. 41695 sites 2nd Gen DRM measurement.

Acknowledgments

This work is funded by the French Ministry DGE in the frame of the “Important Project of Common European Interest (IPCEI)”.

References

- [1] M. Sellier, “Substrate and Device Engineering for IoT and Automotive”, ECS Trans., vol. 85(8), pp. 3-13, 2018
- [2] A. Khakifirooz et al., “Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications” Proc. VLSI-TSA Conference, pp. 110-111, 2010
- [3] W. Schwarzenbach et al., ECS. Trans., 35(5), pp. 239-245, 2011
- [4] W. Schwarzenbach et al., Solid State Electronics, 117, pp. 2-9, 2016
- [5] P.-E. Acosta-Alba *et al.*, ECS Journal of Solid State Science and Technology 2(9), pp. 357-361 (2013)
- [6] W. Schwarzenbach et al, “Advanced FD-SOI and Beyond Low Temperature SmartCut™ Enables High Density 3D SoC Applications”, J. of the Electron Devices Society, 7, pp. 863-868 (2019)
- [7] J. Auerhammer et al., IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2016