Determination of Fracture Properties of Thin Dielectric Films by Nanoindentation

(support of TF3 and also TF2 in IPCEI)

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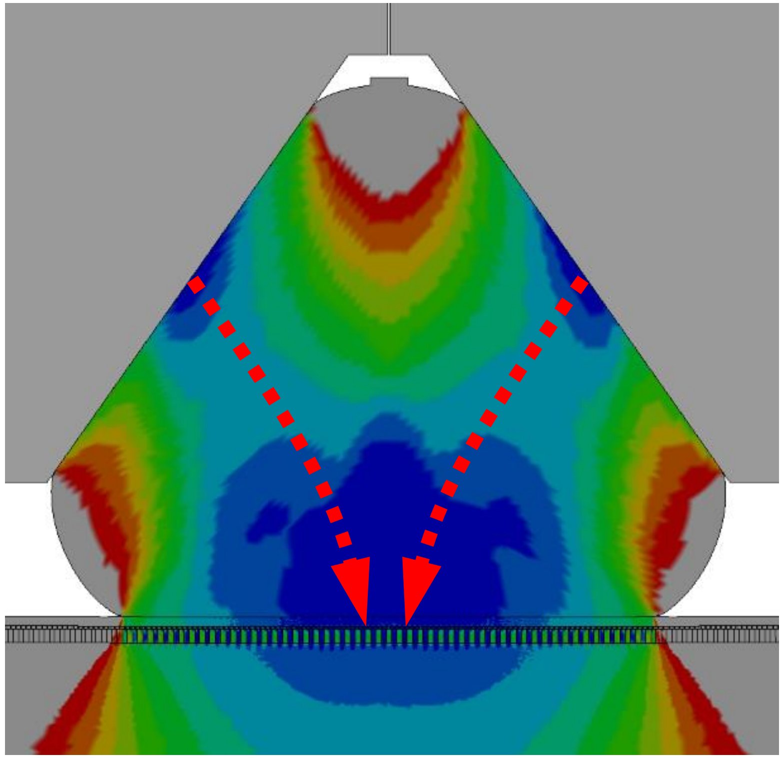
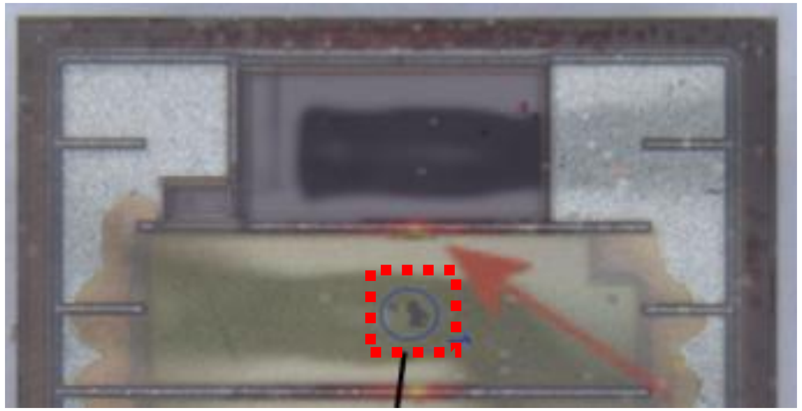
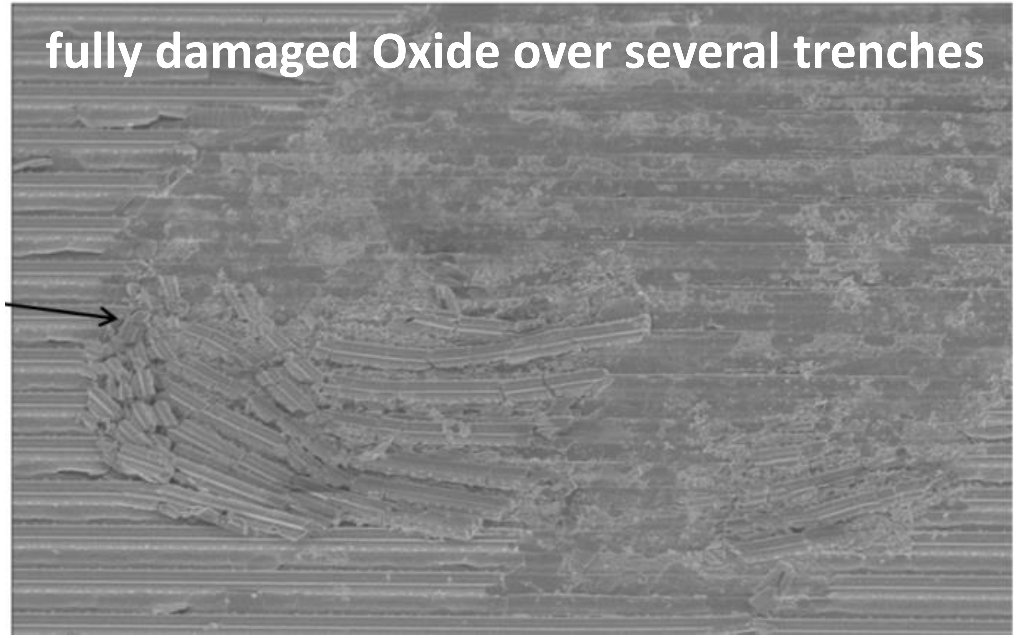
Motivation

Cracking of Oxide, test vehicle#1 MOSFET

- wedge bonding even using the relatively “soft” Al-wire resulted in sever damage of Oxide

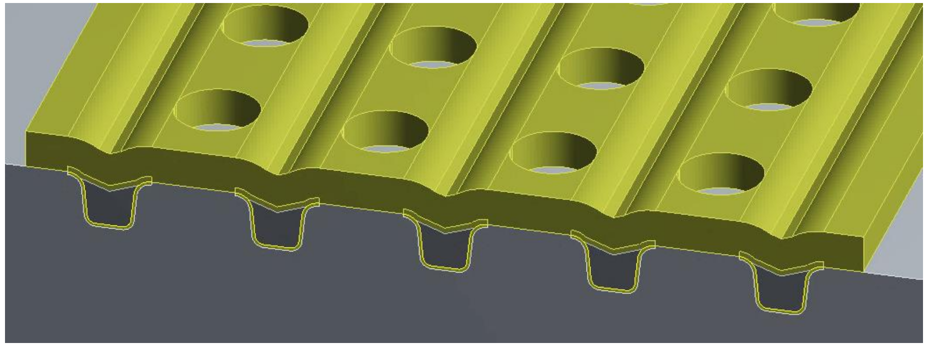


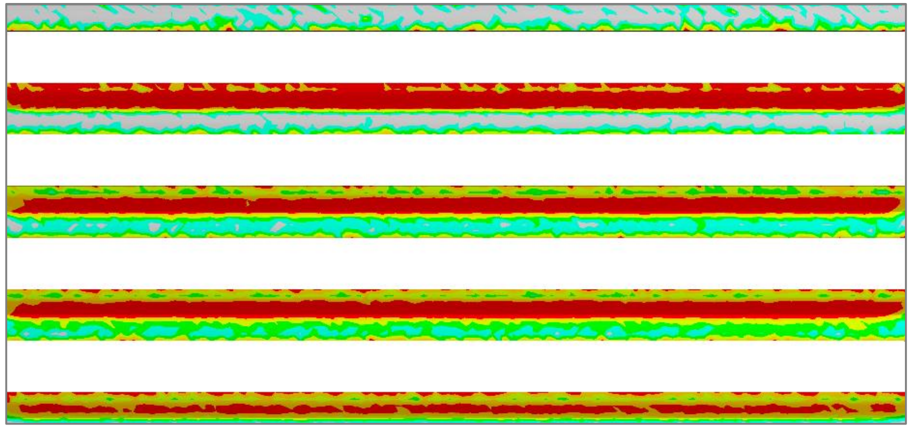


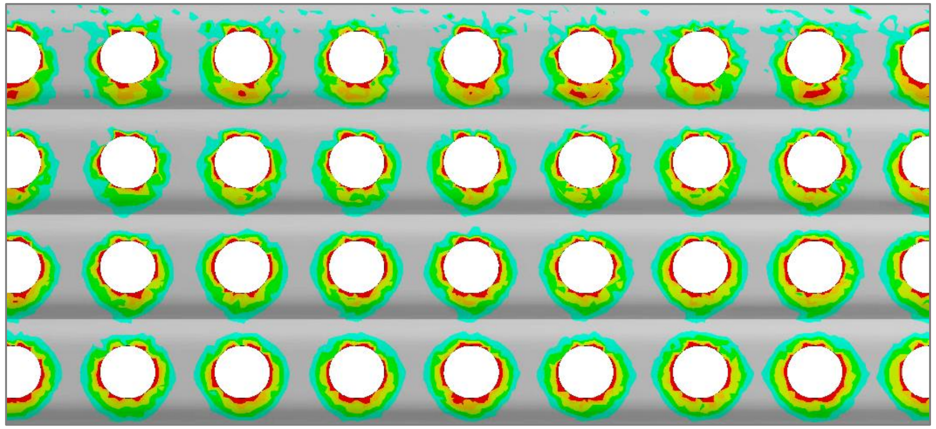


Cracking of Oxide, test vehicle#1 MOSFET

- knowledge of Oxide fracture properties would allow precise quantitative definition improved layout
  - increase of oxide volume effectively improves mechanical stability, but increases electrical resistivity ➔ **qualitative simulation is not enough!**

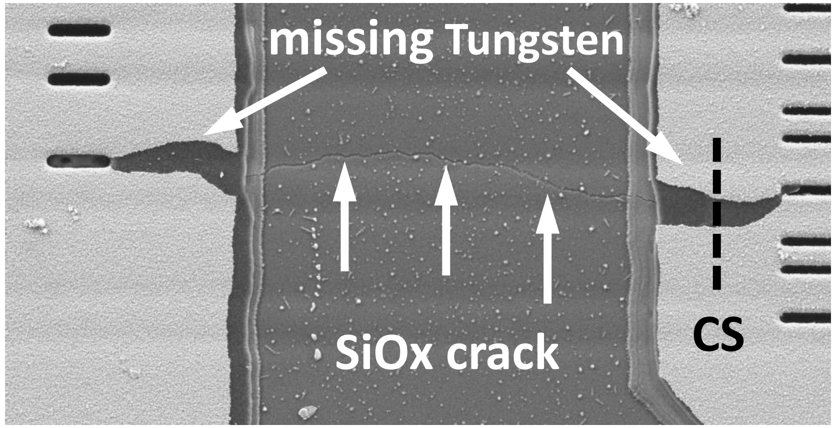


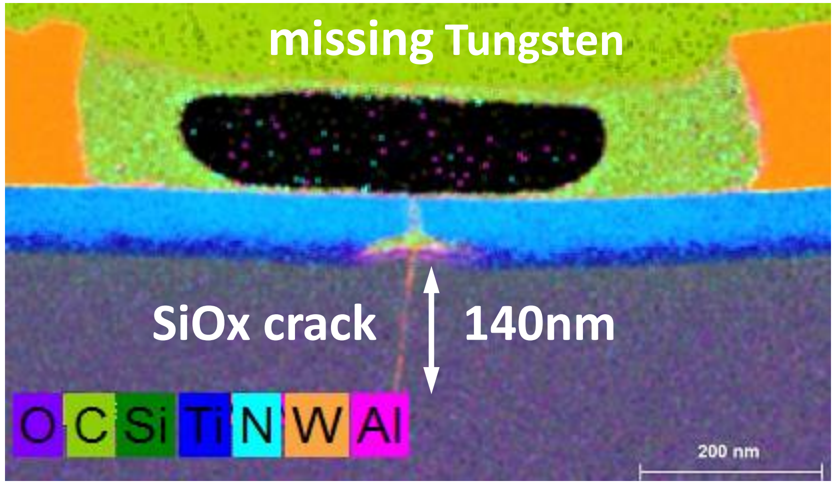




Cracking of Oxide, test vehicle#2: SFET

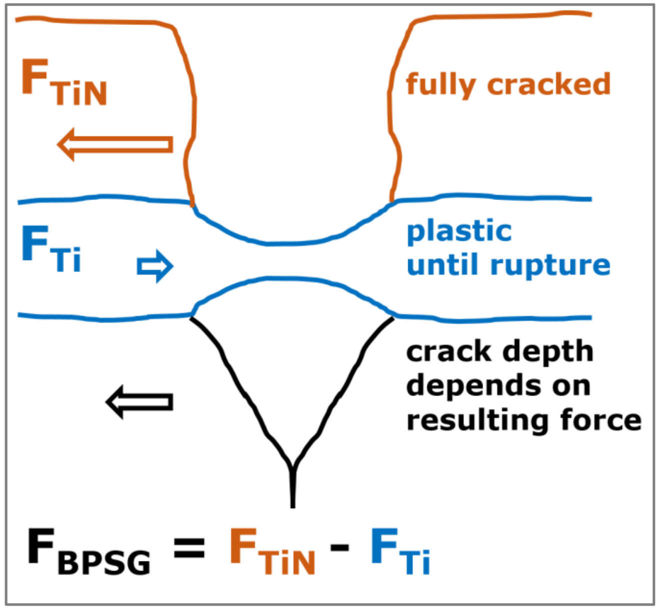
- high risk of local cracking can be induced even by very thin liner (70nm), due to its high stiffness and high intrinsic tensile stress (2GPa)
- crack depth in Oxide is limited, but it opens diffusion path for etching chemistry
    - missing Tungsten affects electrical performance (resistance) of SFET device

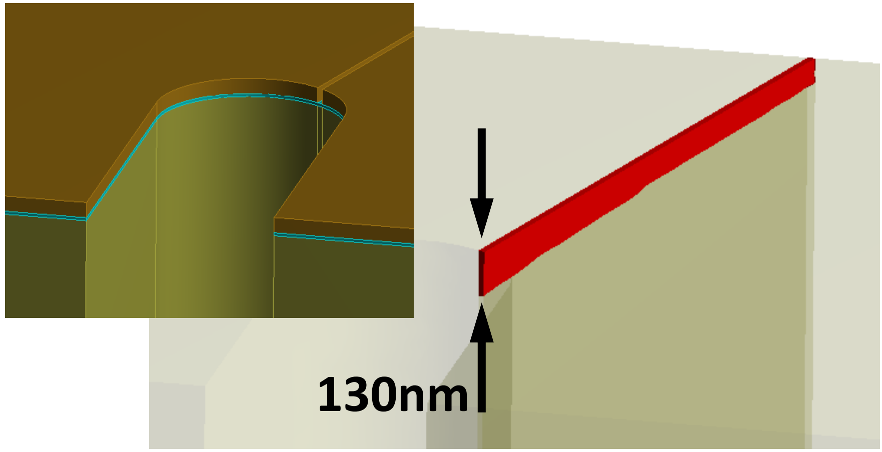




Cracking of Oxide, test vehicle#2: SFET

- knowledge of fracture properties of Oxide would allow predictive simulation of crack depth and precise definition of counter measures
- how far can annealing temperature of Ti/TiN be reduced to avoid cracking?
  - too low annealing temperature would prevent building of TiSi and no electrical contact will be established ➔ **qualitative simulation is not enough!**
- how thin remaining Ti layer can be to avoid cracking?
  - Ti thickness is defined by initial thickness, annealing temperature and duration (nitridation reaction)

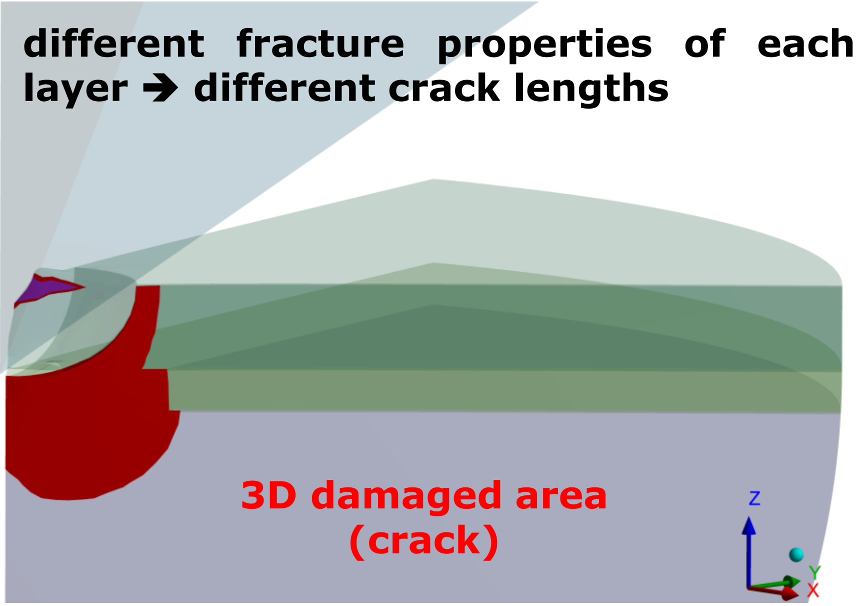


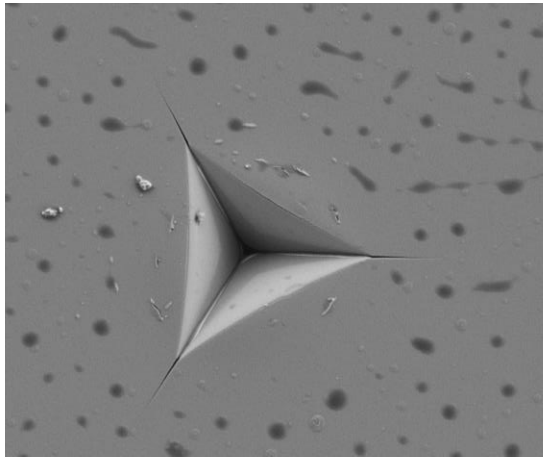


Approach

General

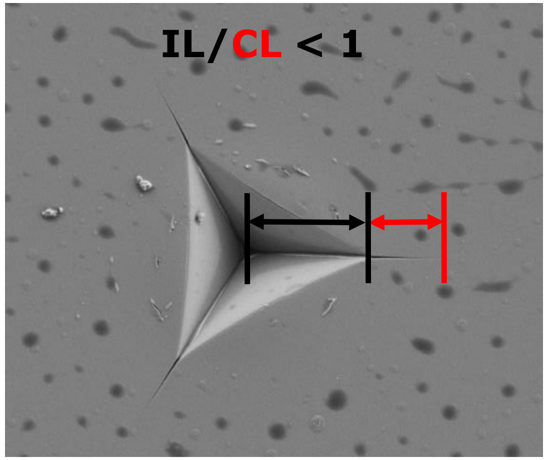
- simulation of crack length for different indentor force levels allows determination of fracture properties of thin brittle layers
  - model parameters are fitted for one force level and verified for other levels
- no restrictions on in how many layers crack can propagate
  - only one layer with unknown properties
- intrinsic layer stress is explicitly taken into account

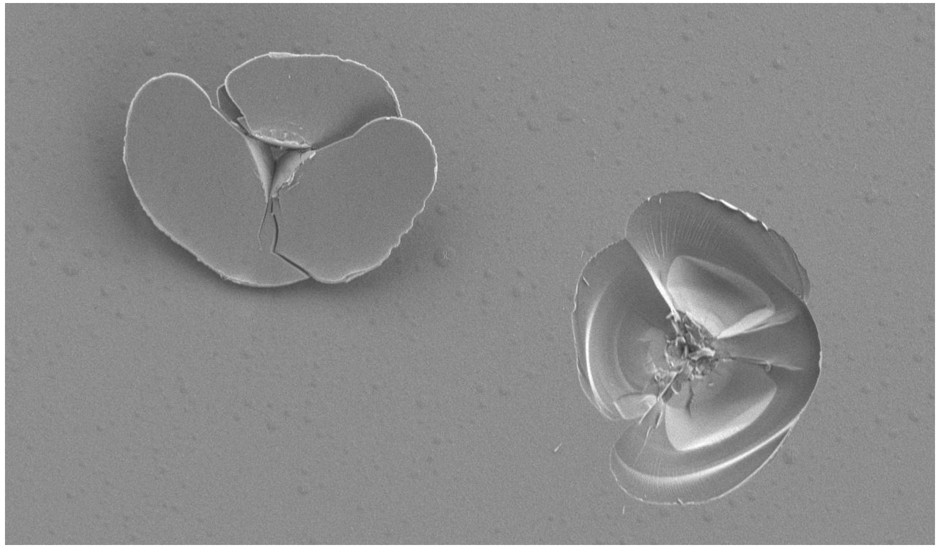




Challenges

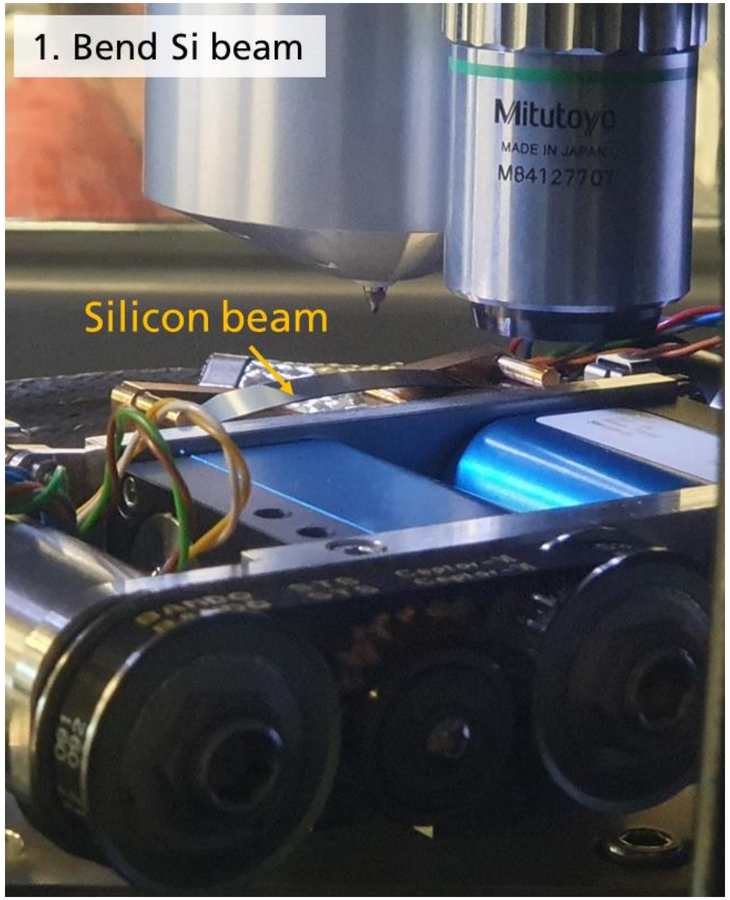
- significant compressive intrinsic stress in Oxide: up to 300MPa
- crack length is too small for reliable determination fracture properties or does not grow at all
  - does not mean that oxide is ductile! ☺
- large chipping, which requires much more complex simulation due to 3D curved cracks

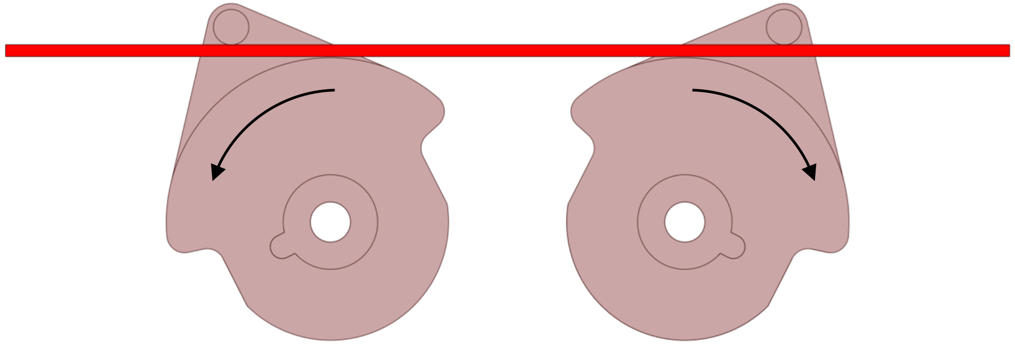


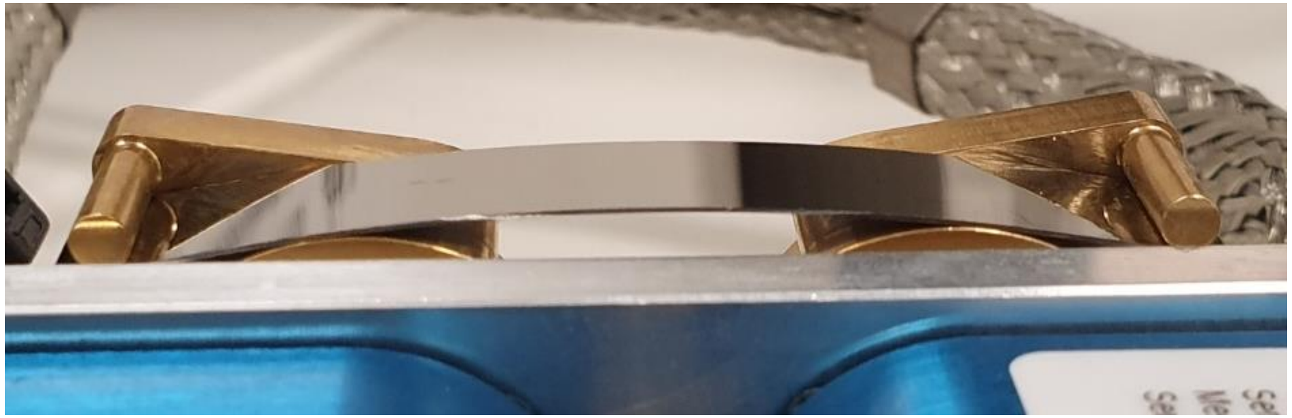


Solution: bent sample

- reduce intrinsic compressive stress by bending

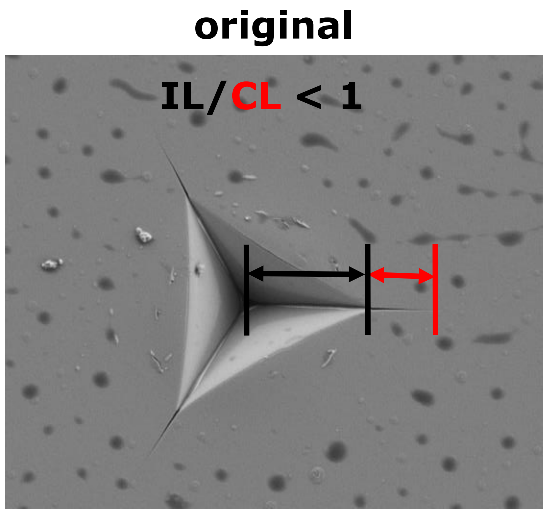


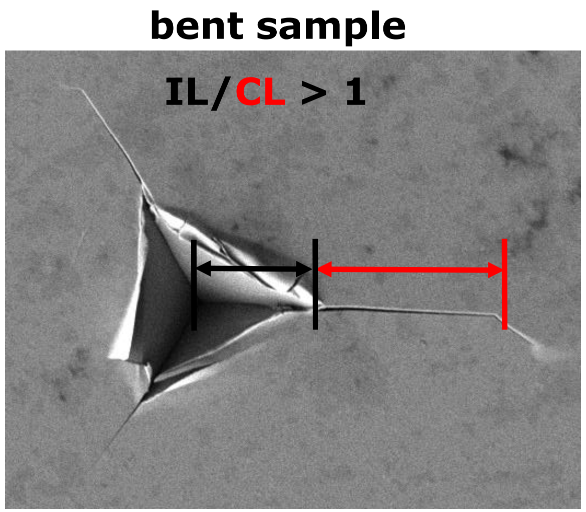


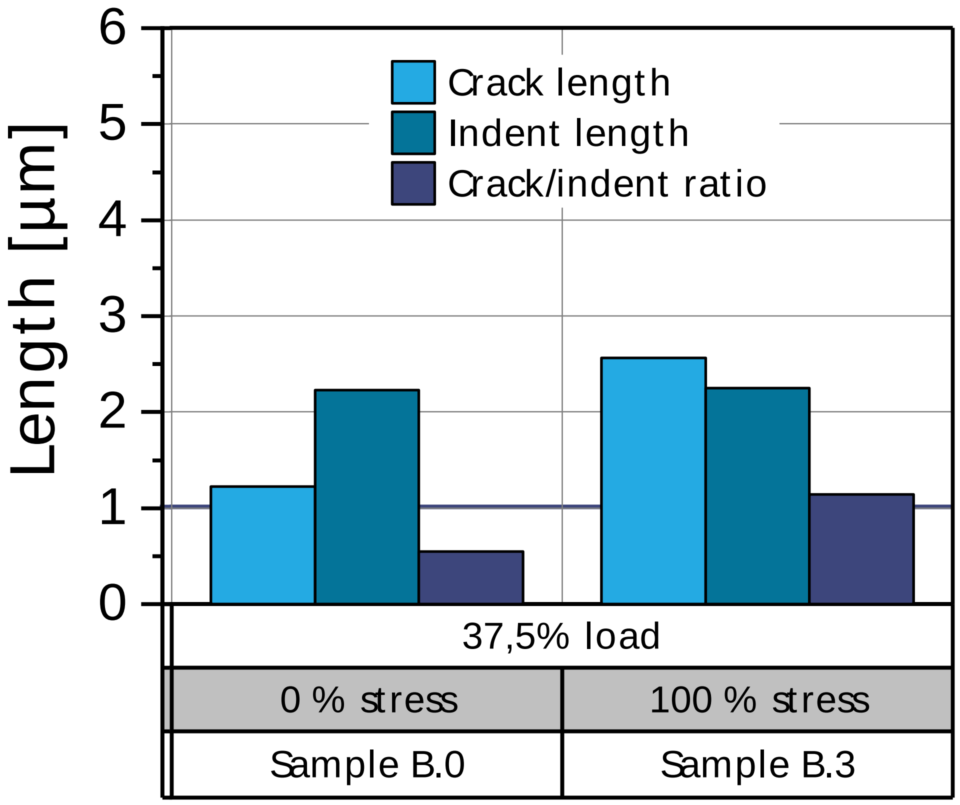


Solution: bent sample

- doubling of crack length for bent sample
- improved relation between indent length and crack length (>1)
  - improvement is seen in the direction of compressive stress reduction by bending

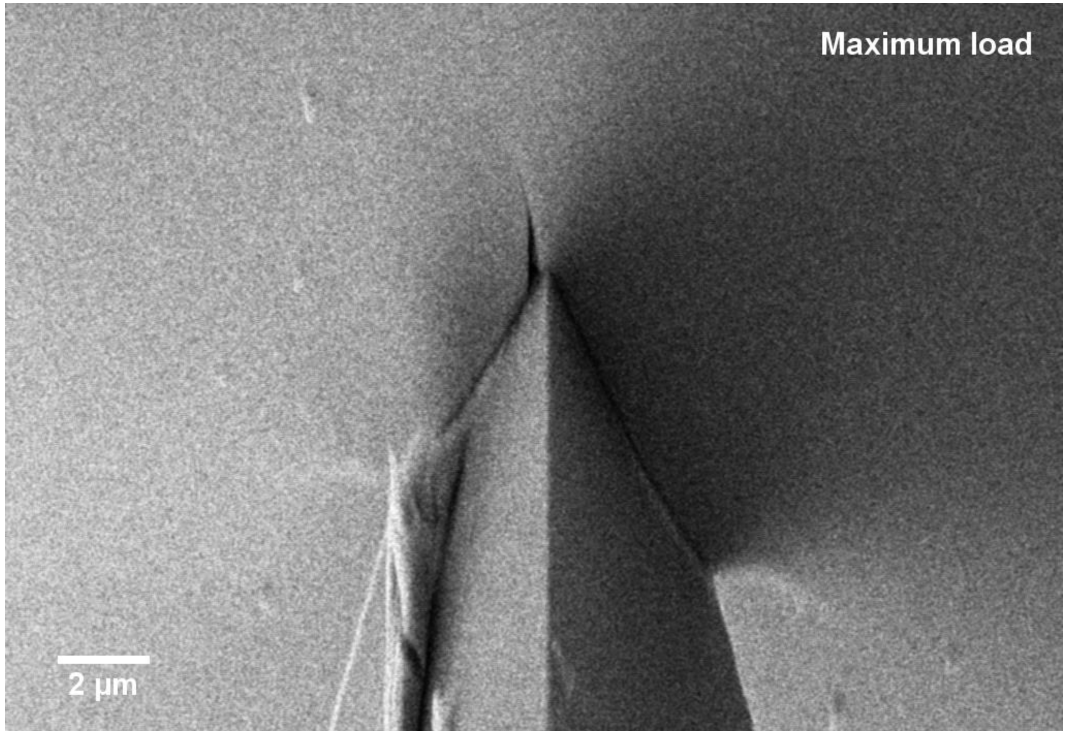






Solution: in-situ indentation

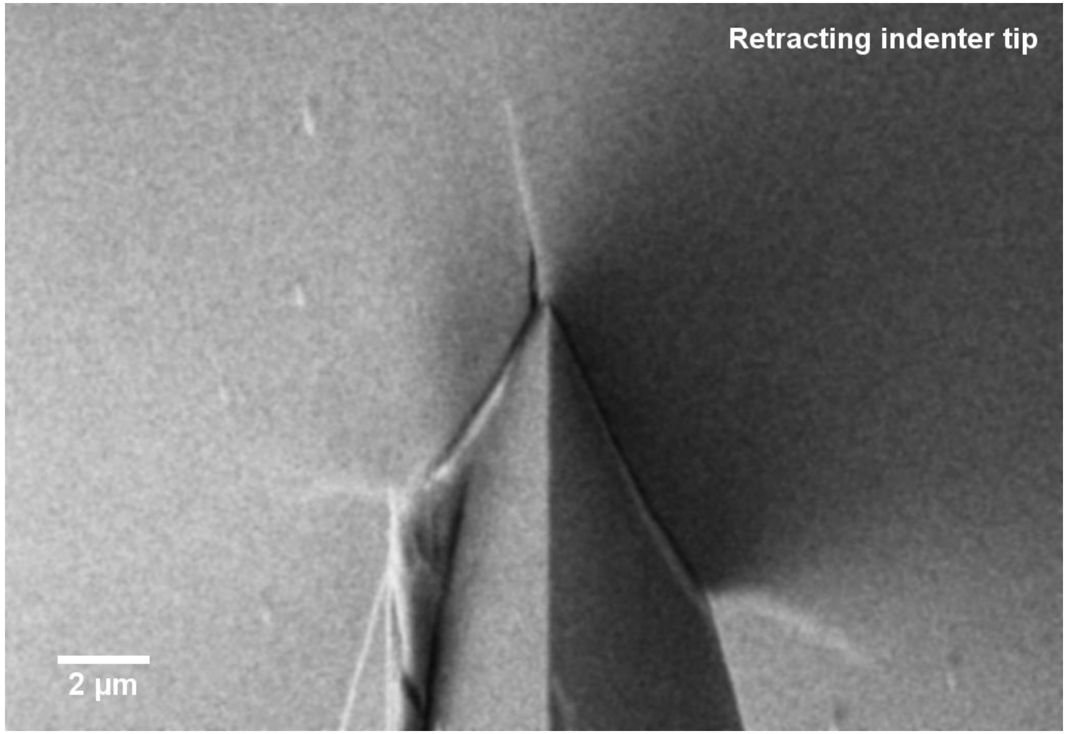
- in-situ SEM indentation allows to measure crack growth “live” during loading <u>and unloading</u>

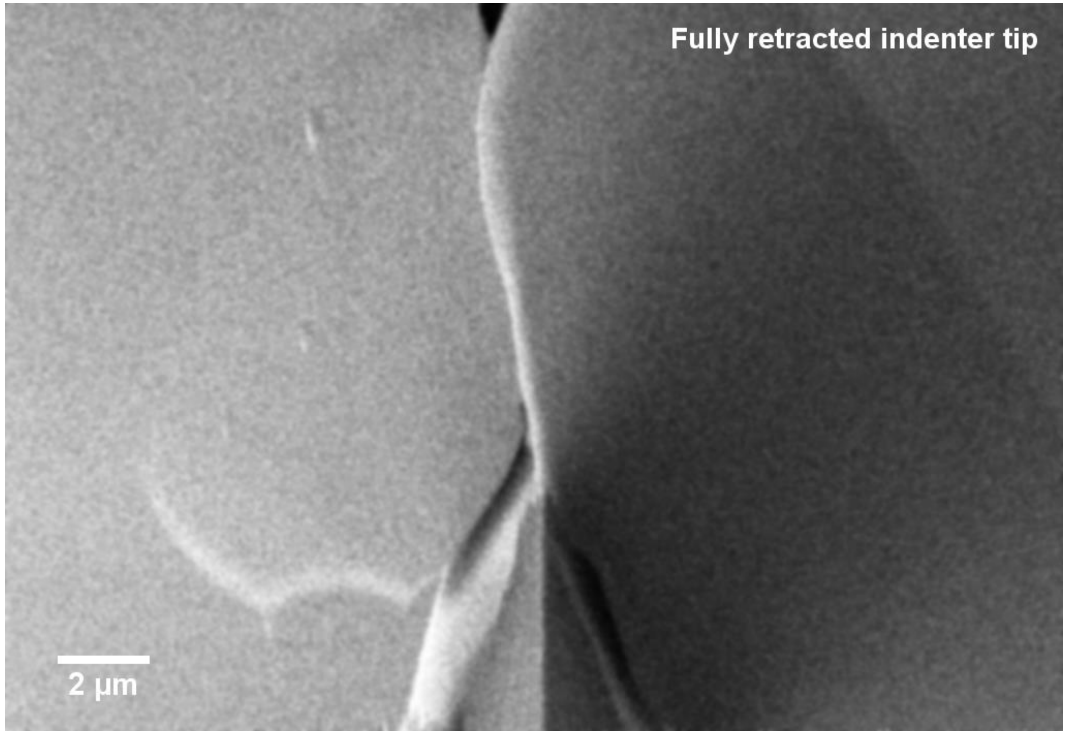


Zwick/Roell ZHN/SEM - Nanoindenter

Solution: in-situ indentation

- large area chipping during unloading
  - stable crack growth during loading
- allowed to test highly brittle/unstable layers





Summary

- work in progress!
- several challenges were successfully resolved so far:
  - compensate effect of large intrinsic compressive stress
  - measure stable crack growth before chipping
- validated simulation models for crack growth will allow to avoid over-engineering in design of robust micro-electronic structures

Thank you

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