“Thermal-electric modelling of thermoelectric and electrocaloric on-chip cooling devices”

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New BEOL-functionality: Temperature Sensing & Manipulation

Challenge: high temperatures adversely affect IC reliability & degrade system performance

Aim: high reliability & efficient regulatory cycles through **Temperature Sensing & Manipulation**

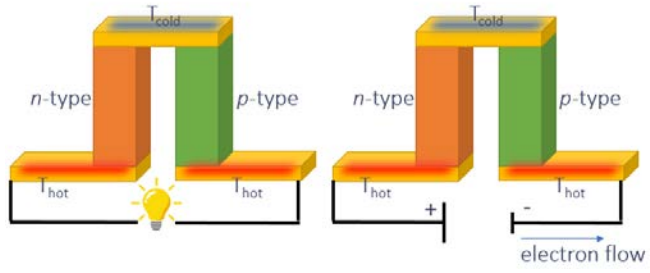
- Development of integration concepts & evaluation of CMOS-compatible materials
- Investigation of pyroelectricity & thermoelectricity concepts as well as their inverse effects
- Evaluation of processes, test structures and characterization methods for potential material & concepts

Thermoelectric

Temperature gradient

↔

Electrical energy

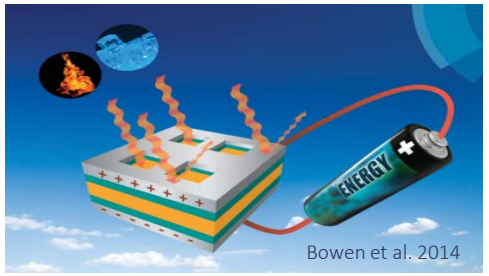


Pyroelectric

Temperature change over time

↔

Electrical energy



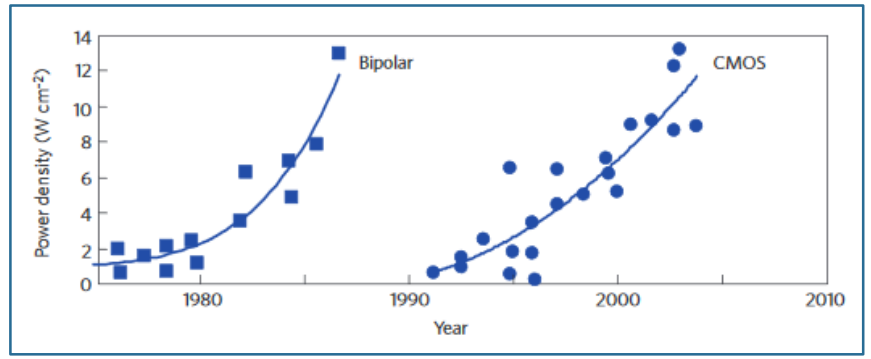
On-Chip Cooling: More Power vs. Waste Heat

Downscaling of CPU → high power density → Hot Spots

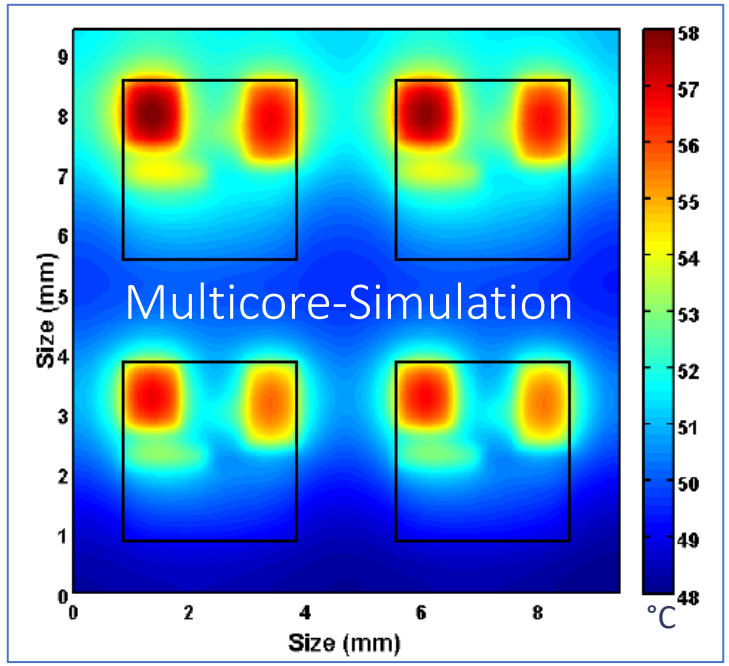
Cooling areas of 1 mm^2 ? →General cooling technologies reach limits (weight, realiability)

Thermoelectric solution?

→active cooling, no moving parts, high reliability, small



A. Majumdar, Nature Nanotechnology, 4 (2009) 214–215.

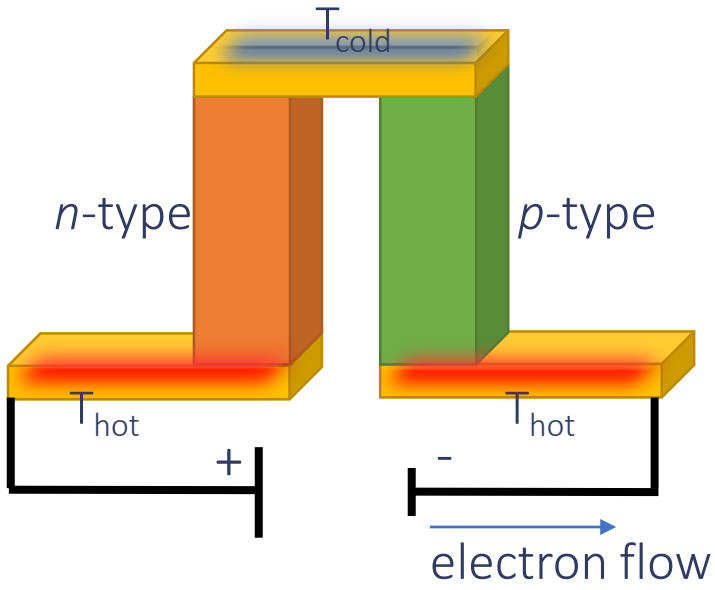


M. Janicki et al, *26th IEEE SEMI-THERM Symposium*, (2010).

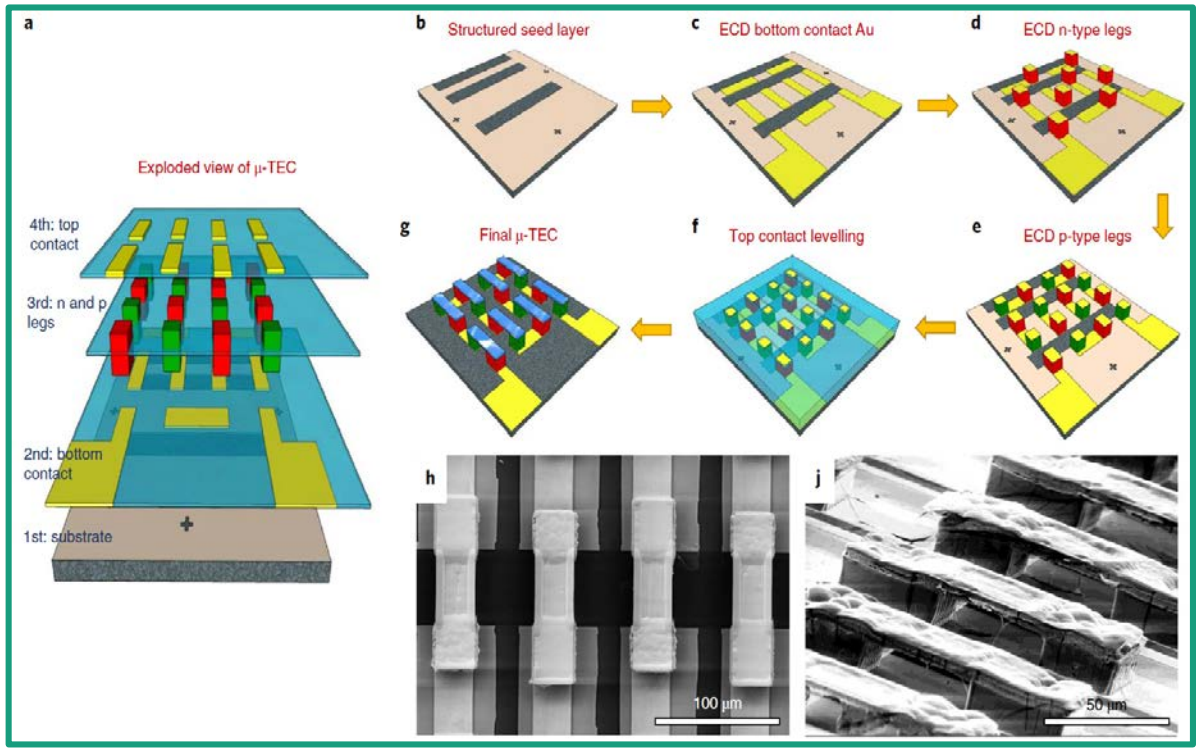
Thermoelectric Basic Principle

Peltier-effect

- Charge carriers transport energy/heat
- Material Interfaces: Heat absorption or emission because of different energy level



➡ µm-scaled Device

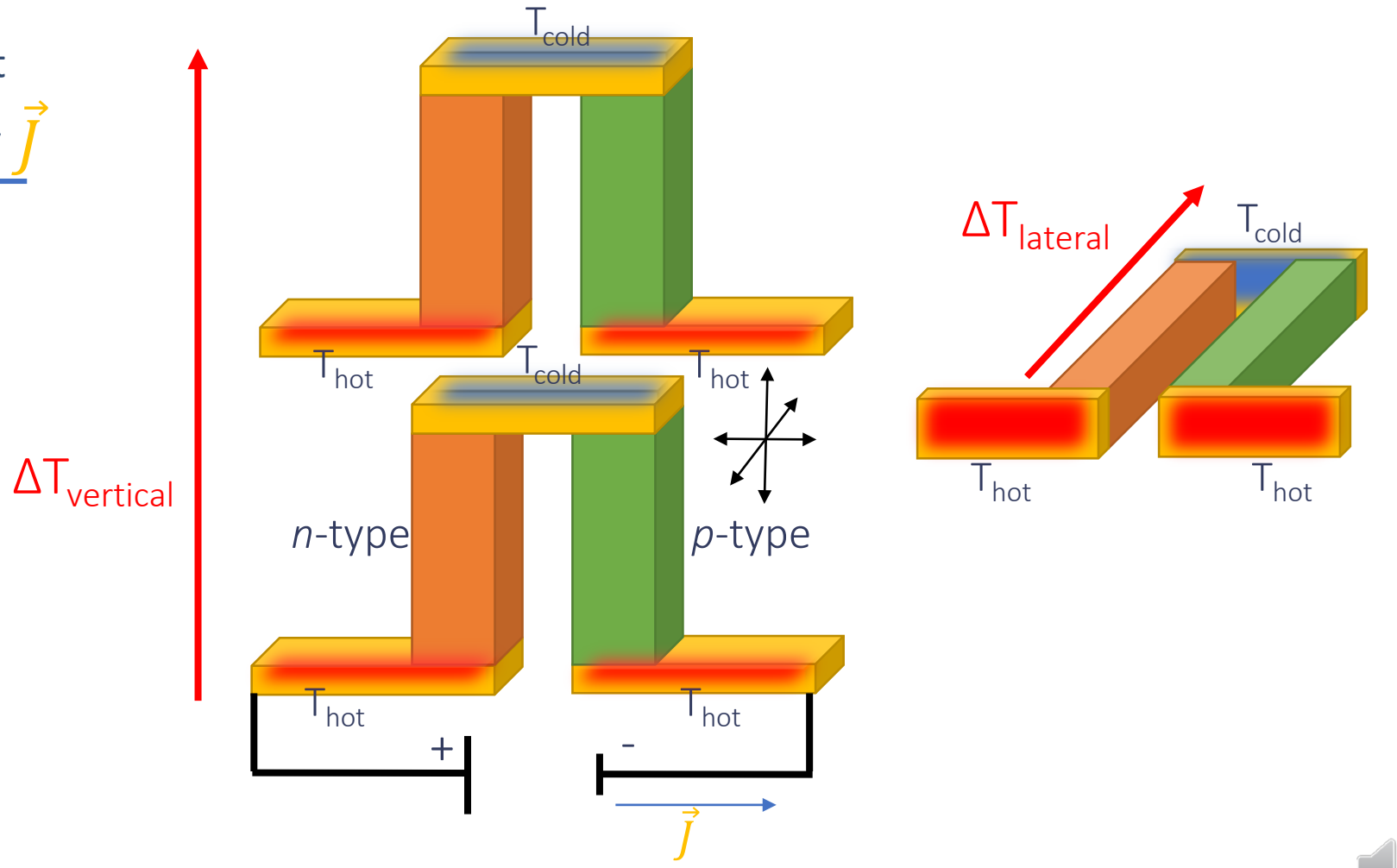


G. Li et al., *Nature Electronics*, 1 **(2018)** 555-561.

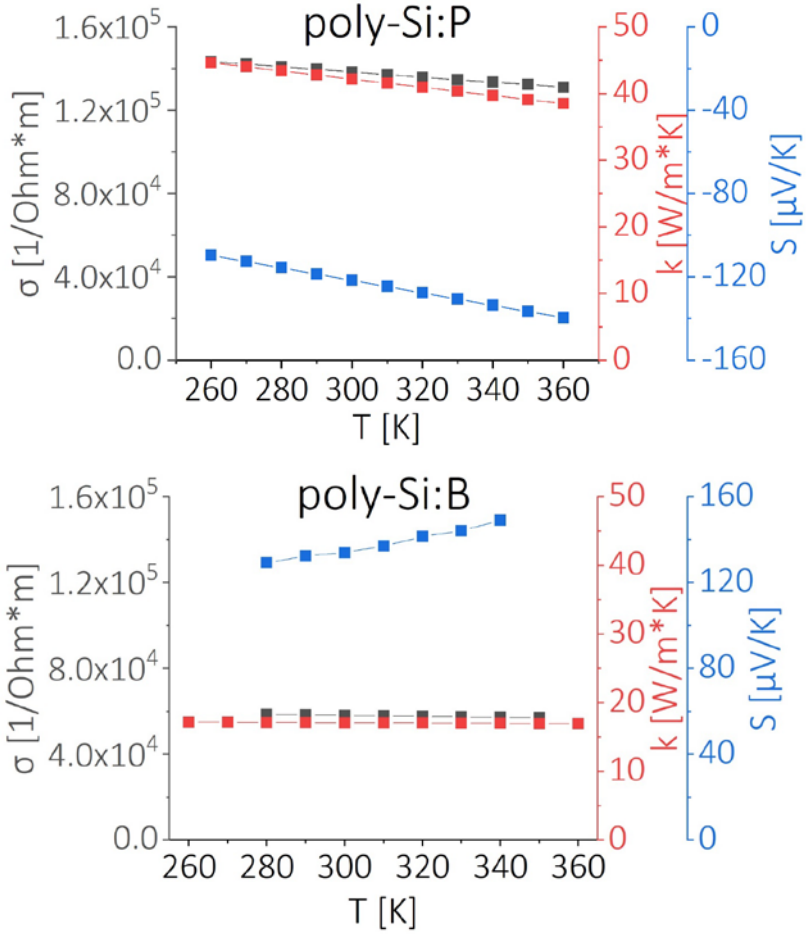
↳ Bi_2Te_3 → not CMOS-compatible

Diversity of Parameters

- Materials (electrode, insulator, TE-material)
- Ambient T of T_{cold} & T_{hot}
- Applied current density $\vec{j}$
- Direction of T-gradient
- Stages
- Dimensions
- Contact resistance

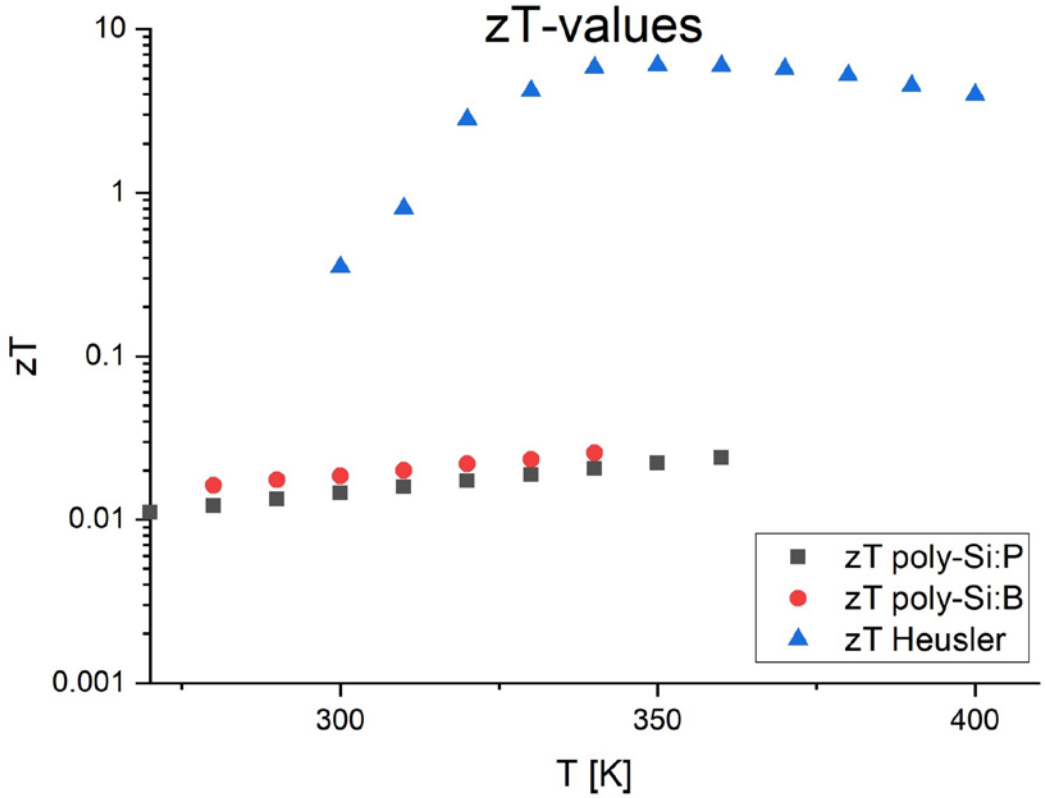


Material data for simulation



J. Calvo et al., *Materials Today: Proceedings*, 5 **(2018)** 10249-10256.

- Experimental data of Boron- & Phosphorous-doped poly-Si
- Comsol material databank used for SiO_2, Si & Cu
- Efficiency of thermoelectric materials:



$$zT = \frac{S^2\sigma}{\kappa}T$$

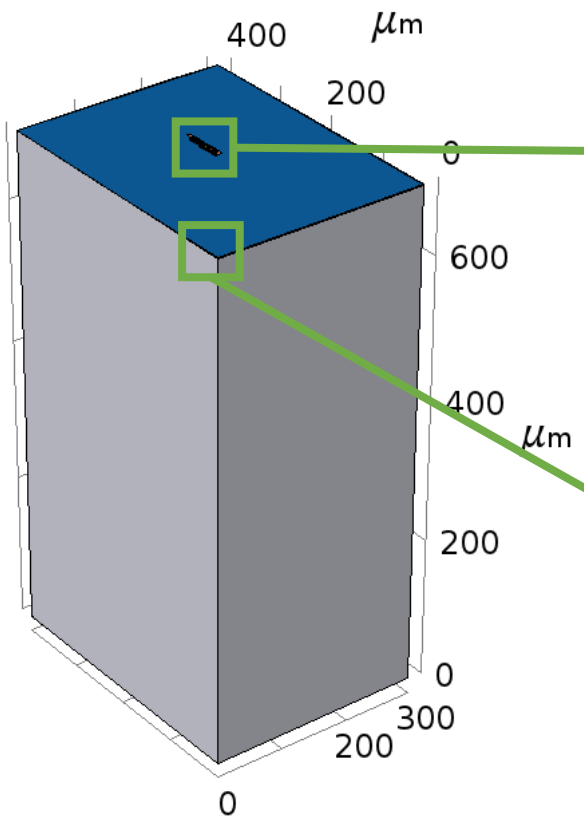
Heusler Compound:
$Fe_2V_{0.8}W_{0.2}Al$

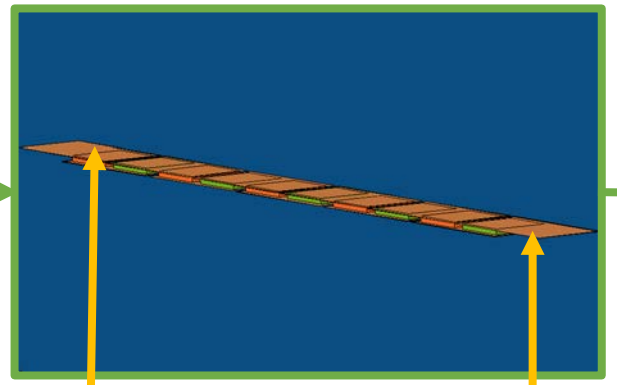
B. Hinterleitner et al., *Nature*, 576 **(2019)** 85-90.

Admont

Thermoelectric: Device Geometry & Physics

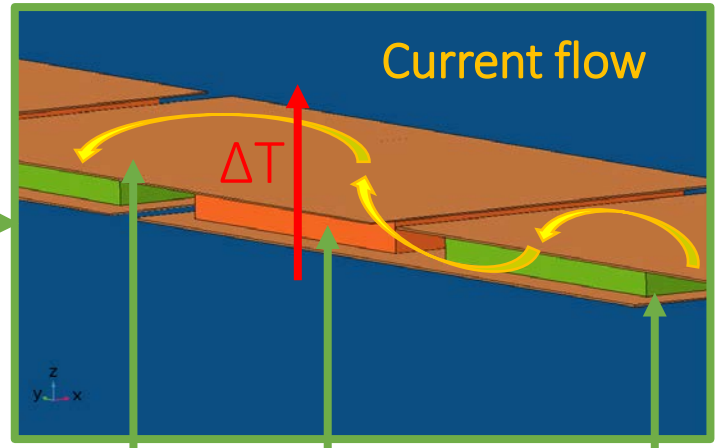
- Vertical ΔT-Gradient





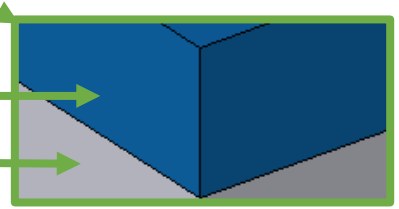
Ground

Current Density $\vec{J}$



Cu-electrode
H:20nm
B:5μm
L:8μm

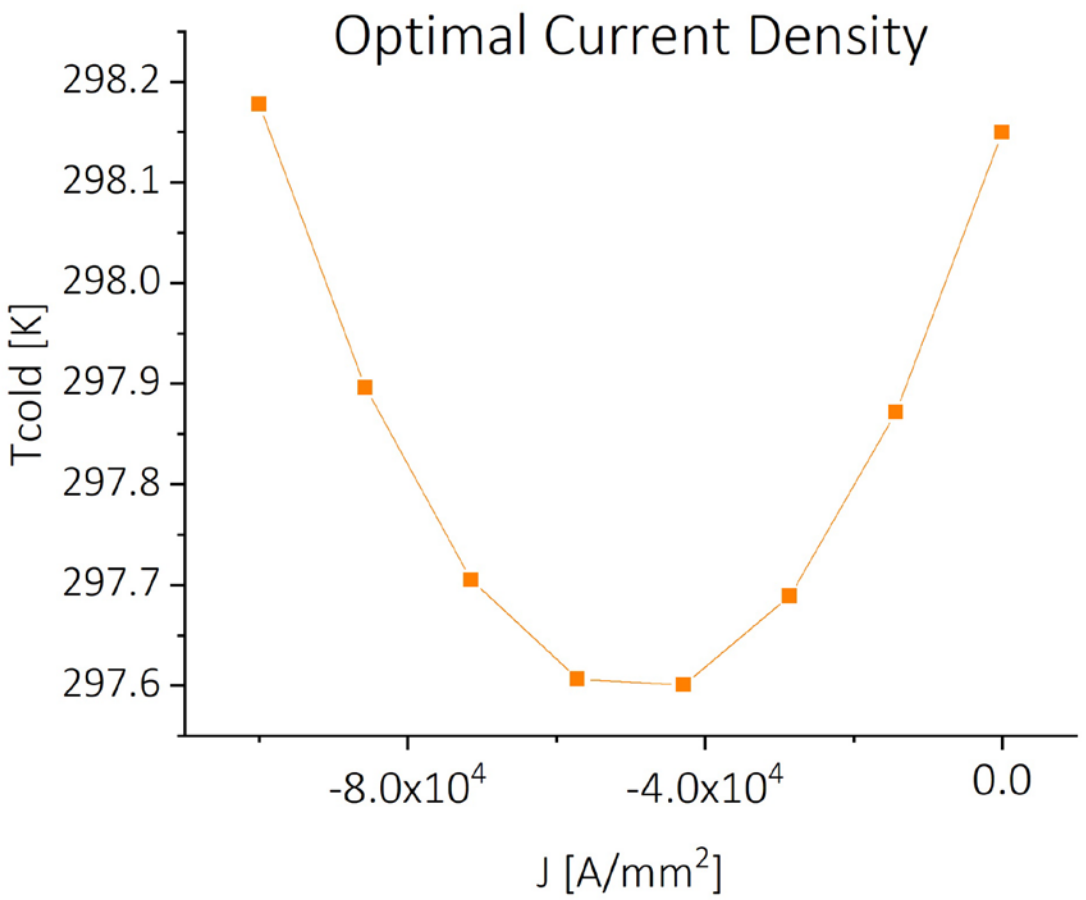
B-doped-leg & P-doped-leg
H:400nm
B:4μm
L:4μm

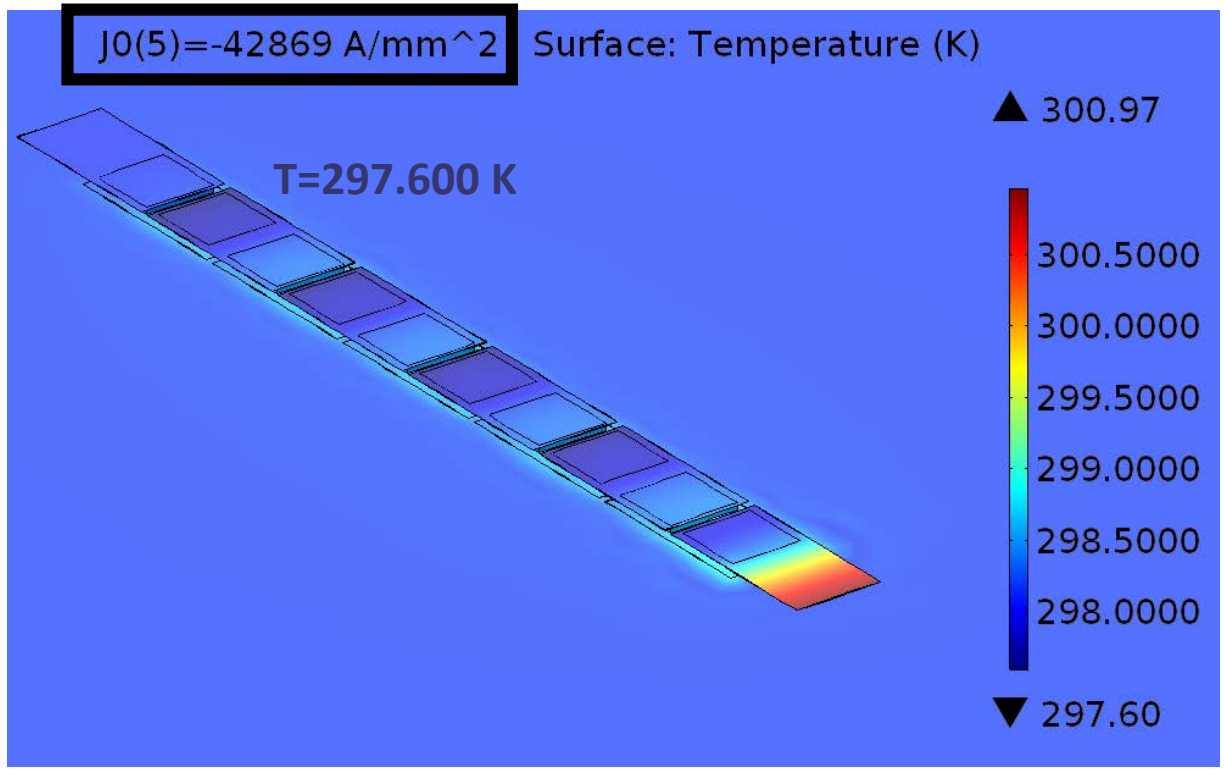


TOX-Substrate (1μm)

Si-Wafer (700μm)

Vertical: COMSOL-Simulation



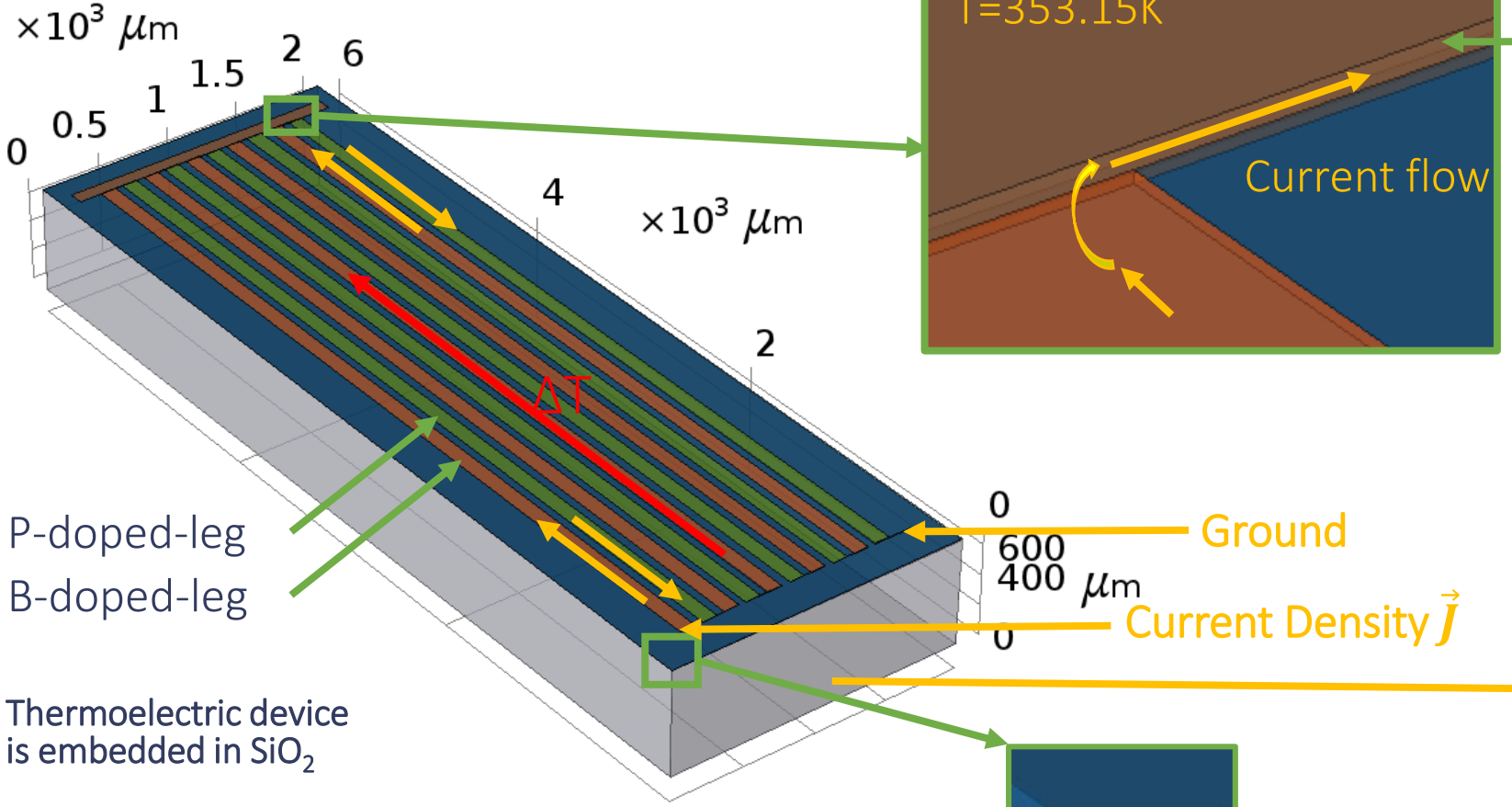


ΔT_{TEC}=298.15-297.60=0.55K → small vertical T-gradient
→ high current density

➡ Could a lateral temperature distribution be better?

Thermoelectric: Device Geometry & Physics

- Lateral ΔT-Gradient



Cu-Hotspot (no current)

Cu-electrode

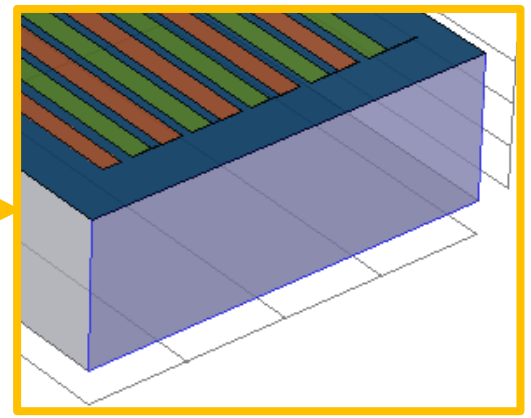
P-doped-leg

B-doped-leg

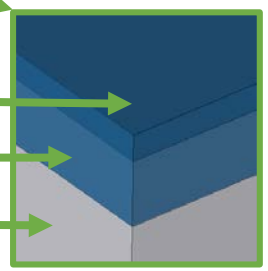
Ground

Current Density $\vec{J}$

Area of Heatsink



Thermoelectric device is embedded in SiO_2

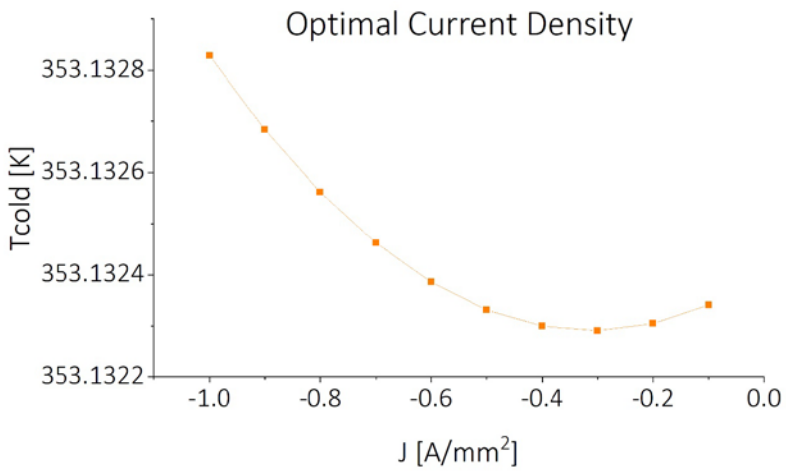


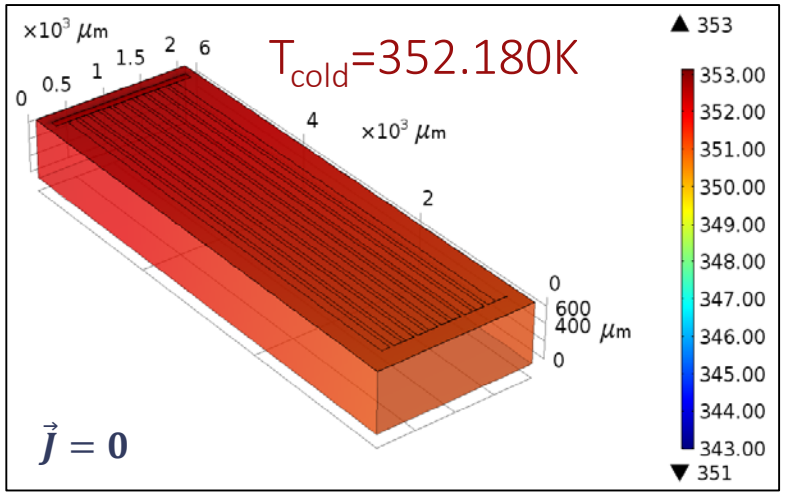
SiO_2-Insulator (400nm)

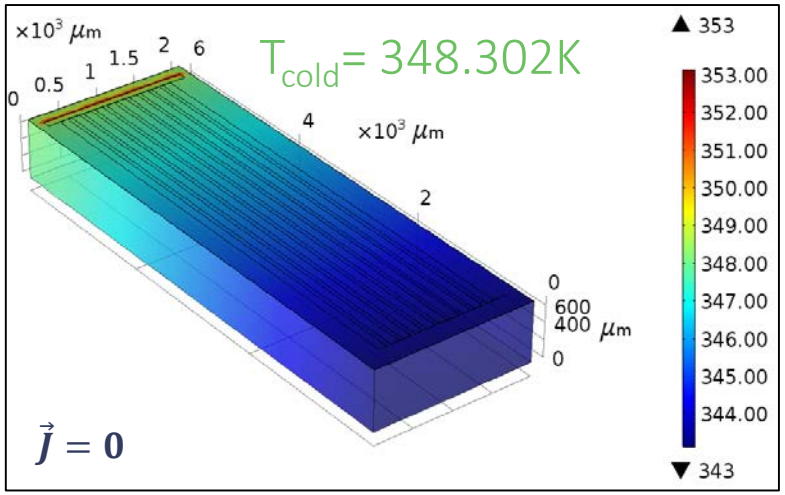
TOX-Substrate (1µm)

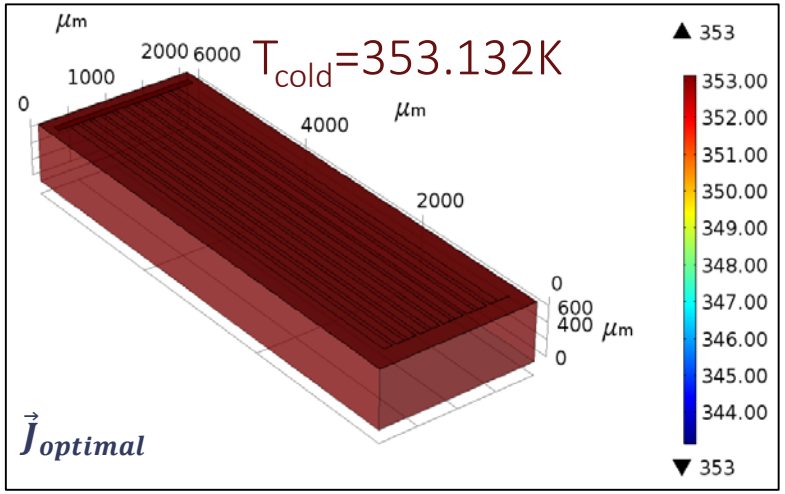
Si-Wafer (700µm)

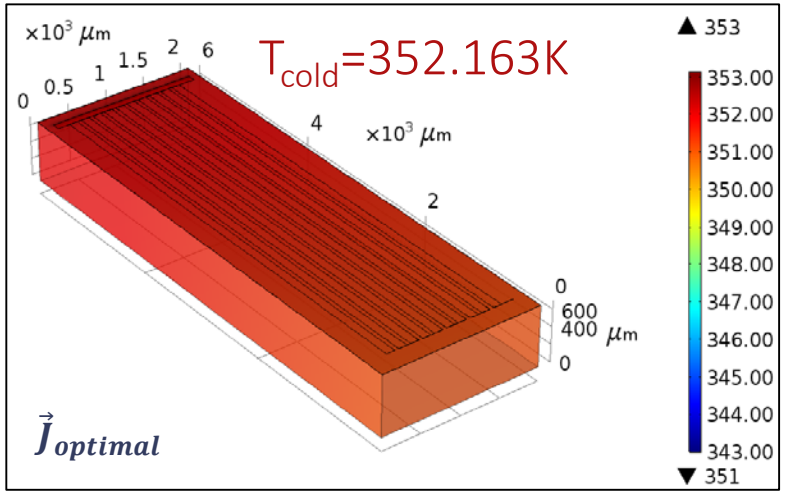
Lateral: Parameter Variation

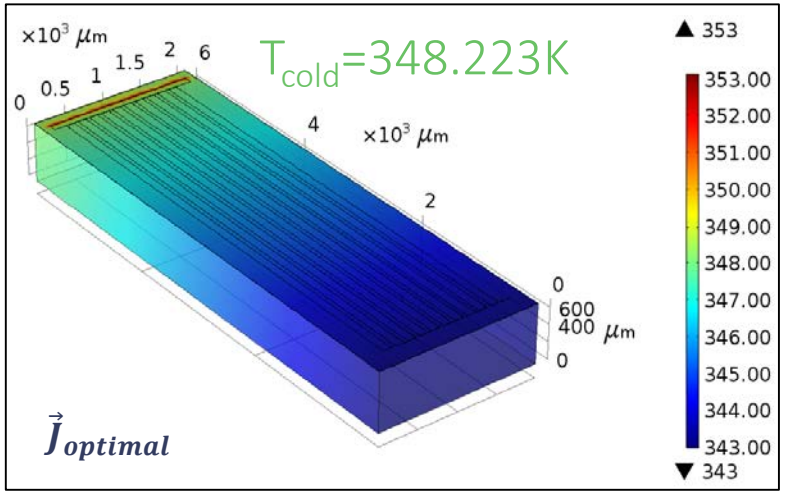












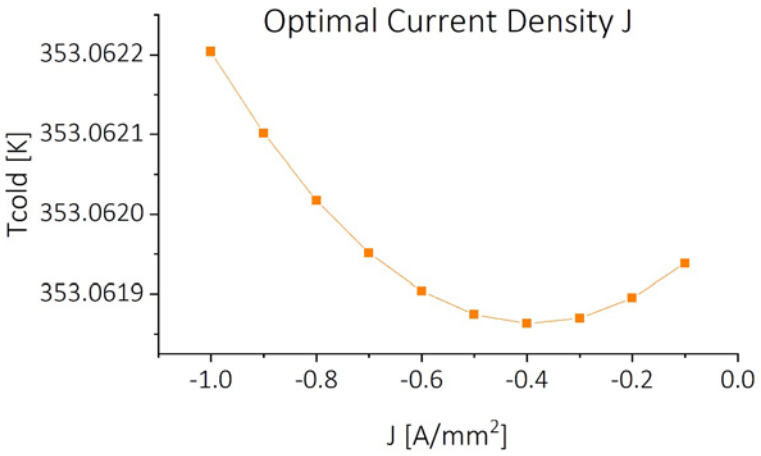
ΔT_{TEC}=0.018K

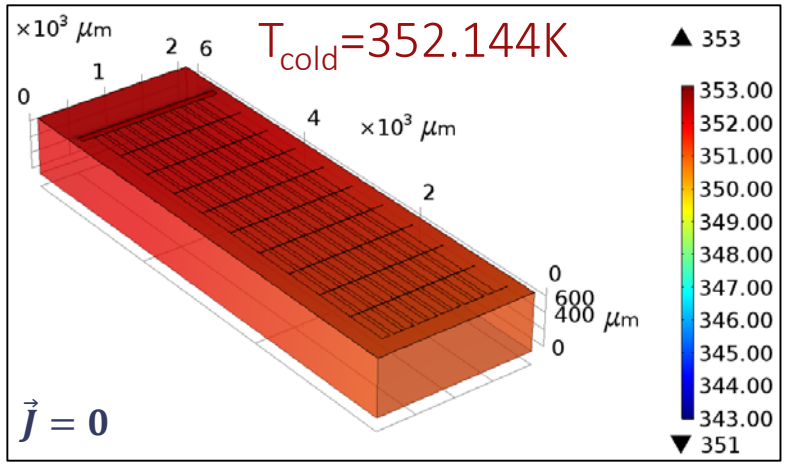
ΔT_{TEC}= 352.180-352.163=0.017K

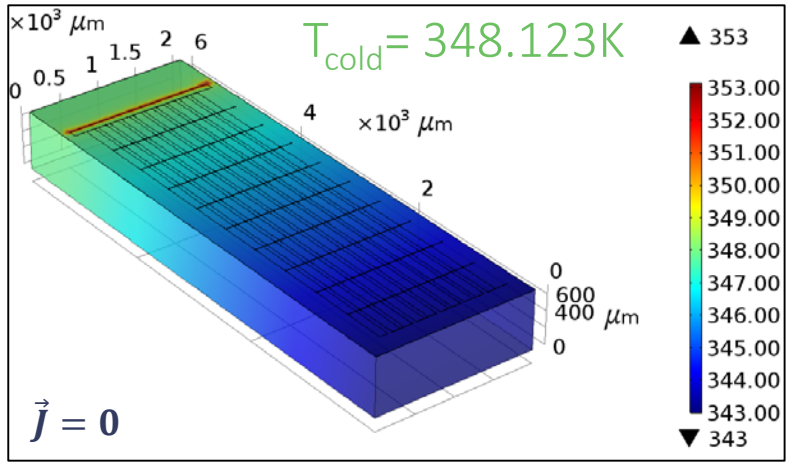
ΔT_{TEC}=348.302-348.223=0.08K

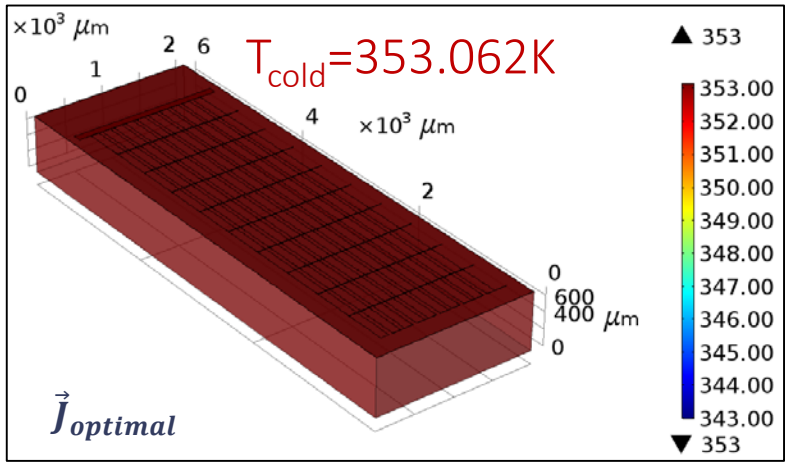
➡ TEC has no significant impact on ΔT

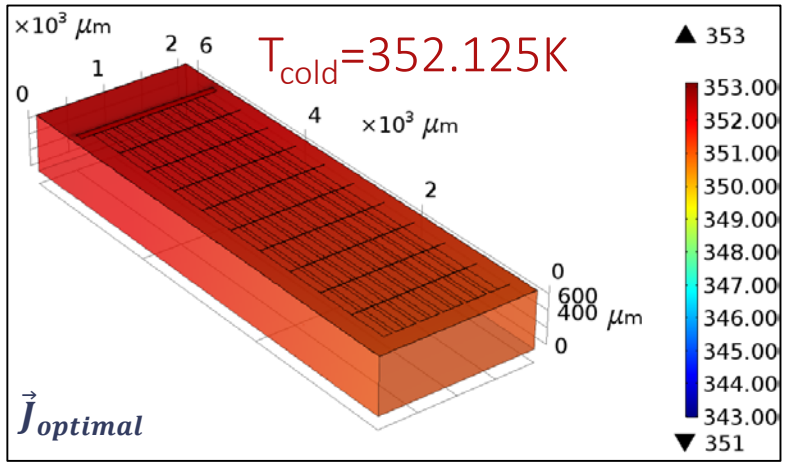
Lateral: Number of Stages

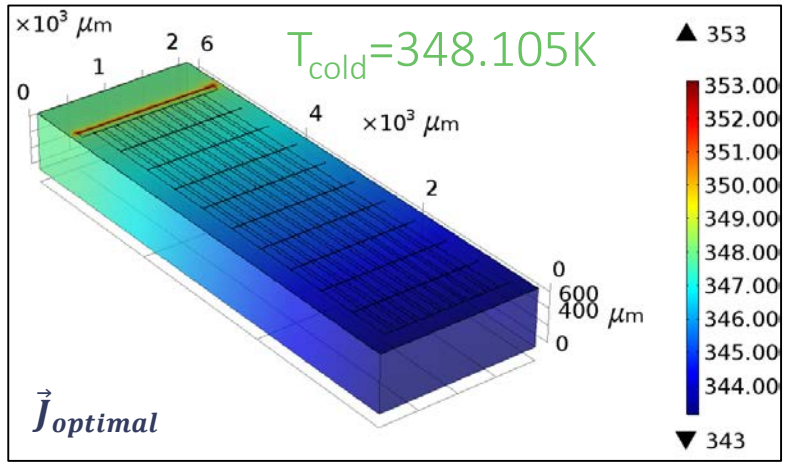












ΔT_{TEC}=0.08K

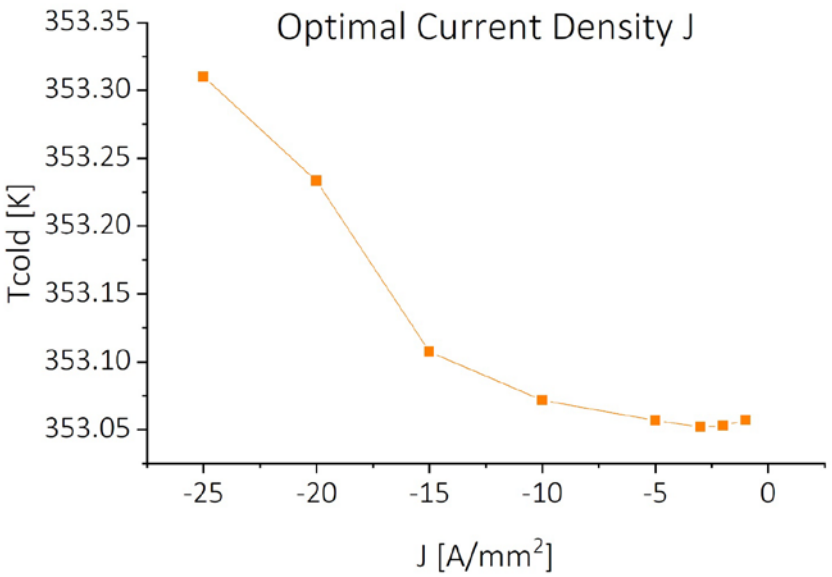
ΔT_{TEC}= 352.144-352.125=0.018K

ΔT_{TEC}= K=348.123K-348.105=0.018K

➡ multistage-TEC has no significant impact on ΔT

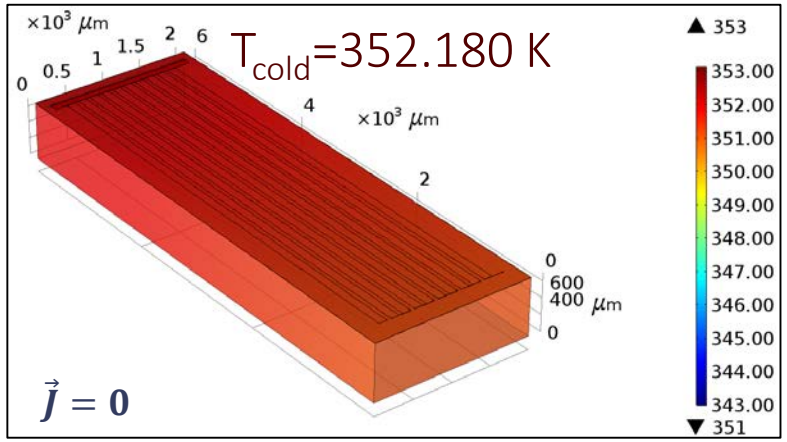
Thermoelectric: state of the art

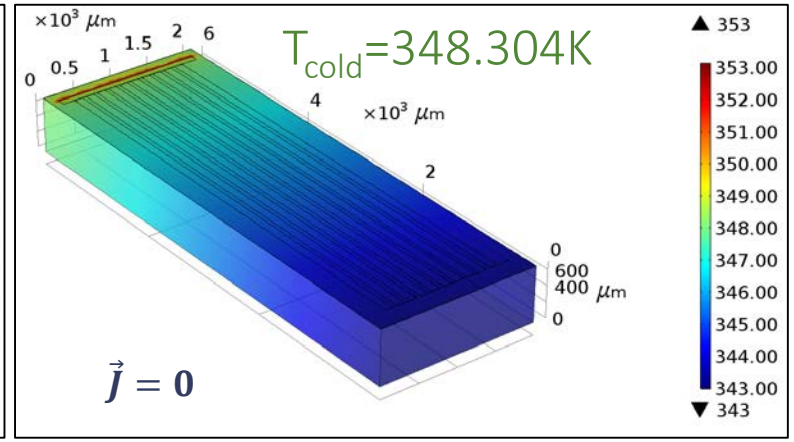
- Heusler compound $Fe_2V_{0.8}W_{0.2}Al$ → best reported zT ≈ 6

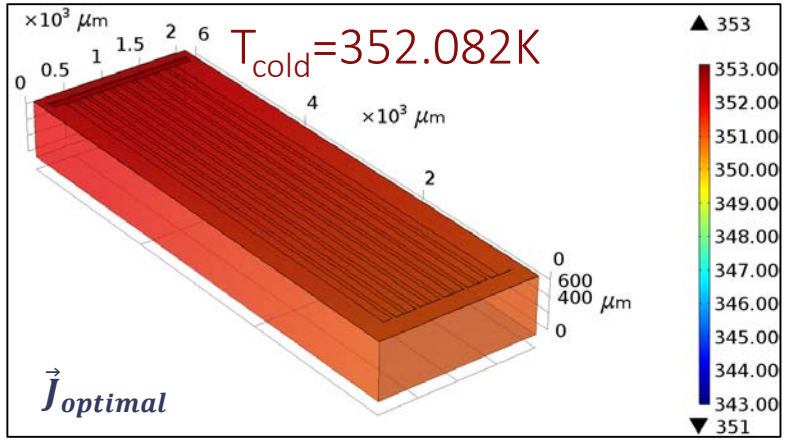


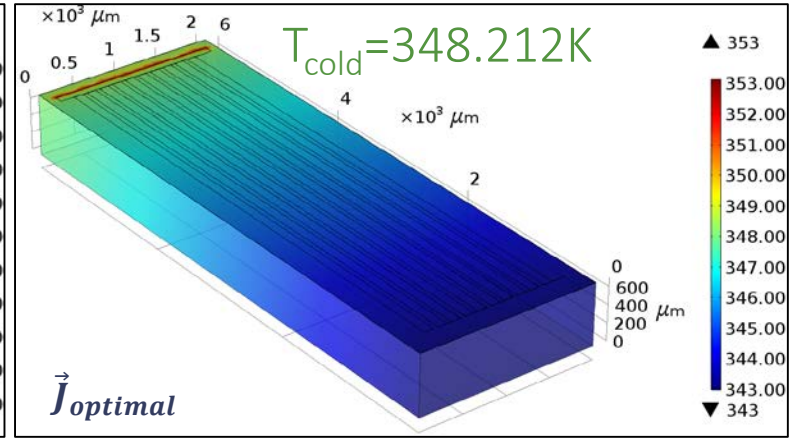
$\vec{J}_{optimal} \approx -3\ A/mm^2$

ΔT=0.1K→ more than 5x higher compared to poly-Si (**ΔT=0.018K**)







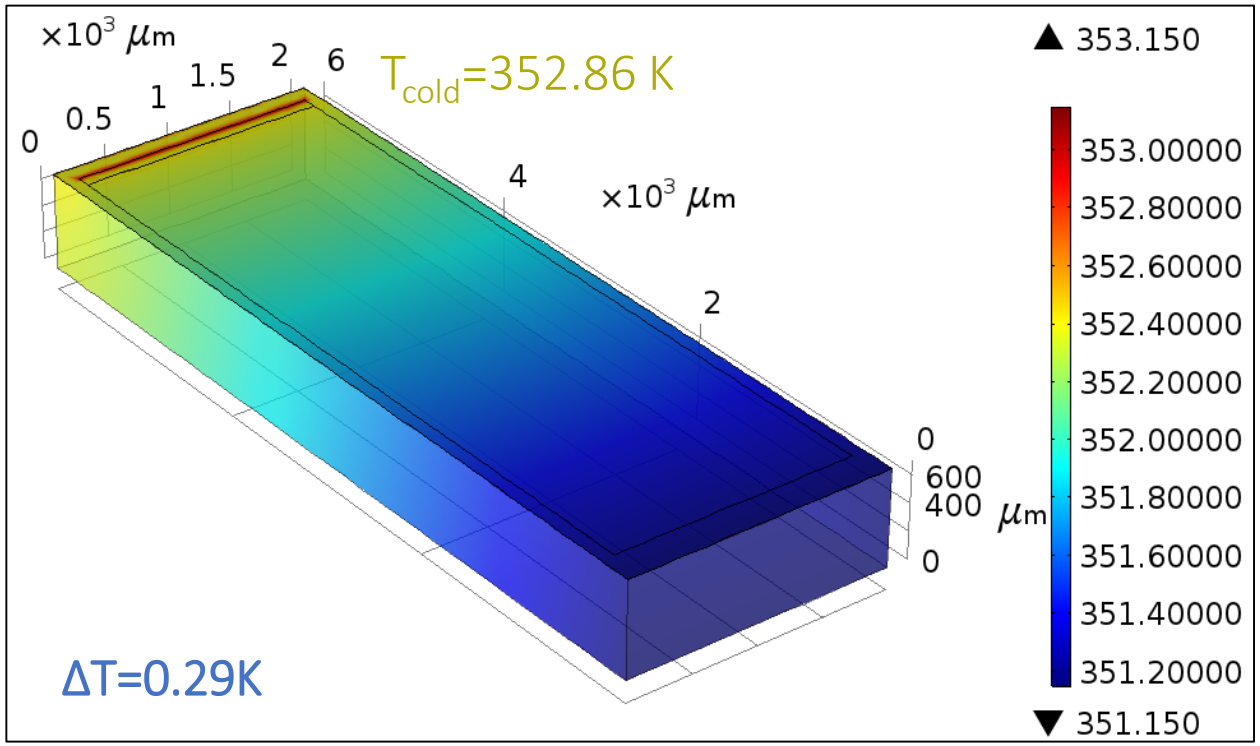


ΔT_{TEC}=352.182-352.082=0.097K

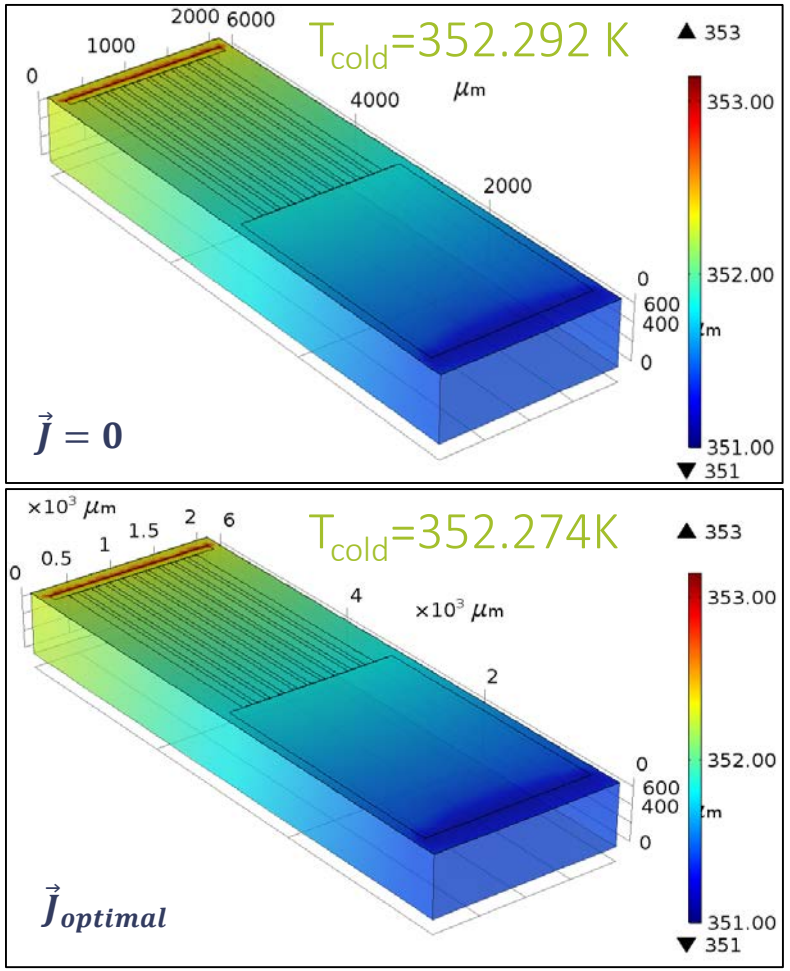
ΔT_{TEC}= 348.304-348.212=0.092K

Lateral: Passive vs. Combination

Passive cooling: Cu heatspreader instead of TEC



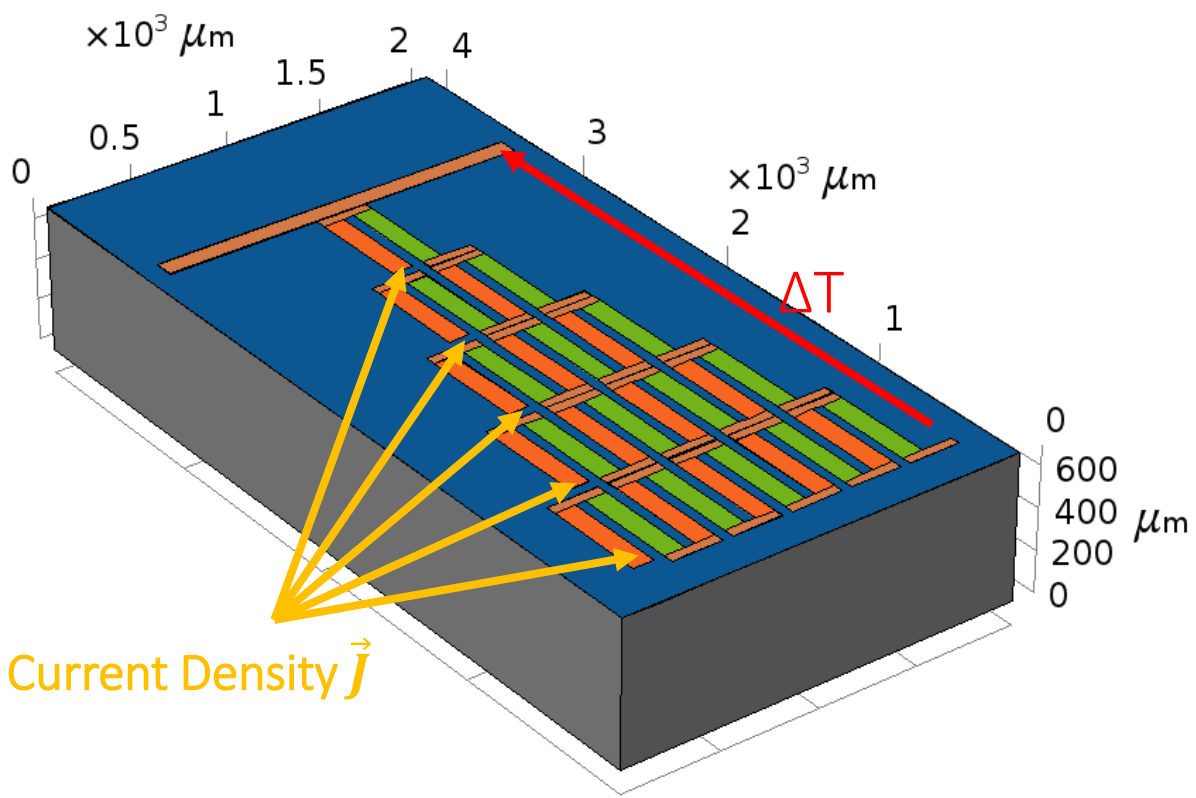
Combination: Cu-heatspreader & TEC

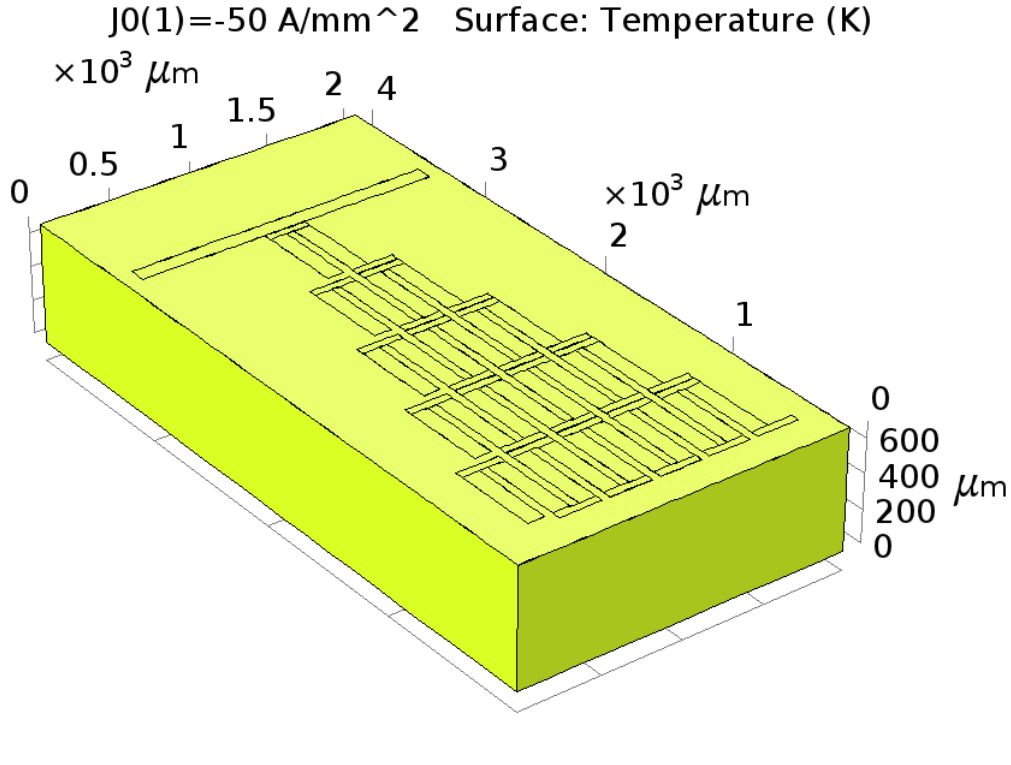


ΔT$_{TEC}$=352.292-352.274=0.018K

➡ Cu-heatspreader has an higher impact on ΔT than TEC

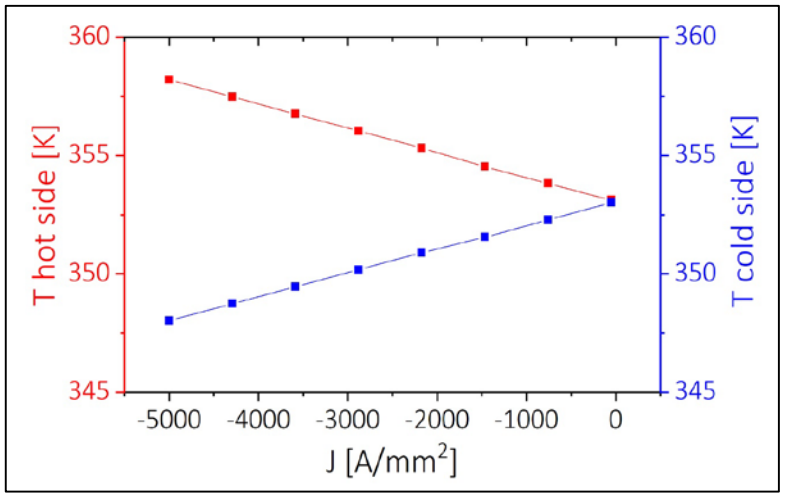
Lateral: Pyramidal Structure

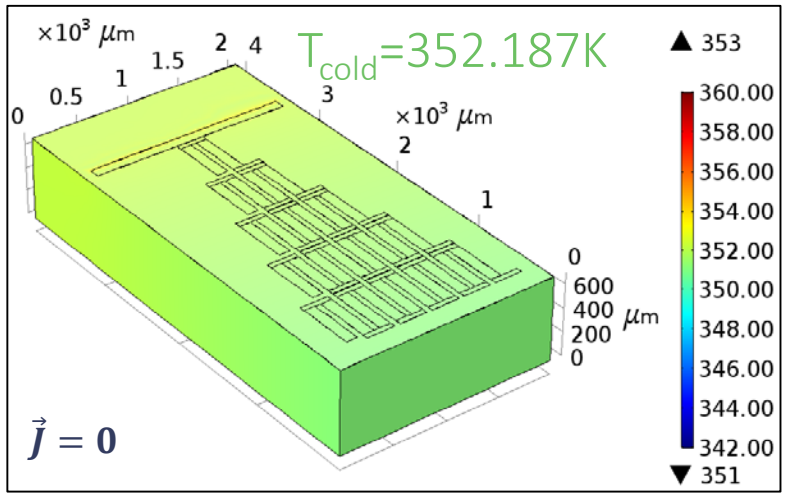


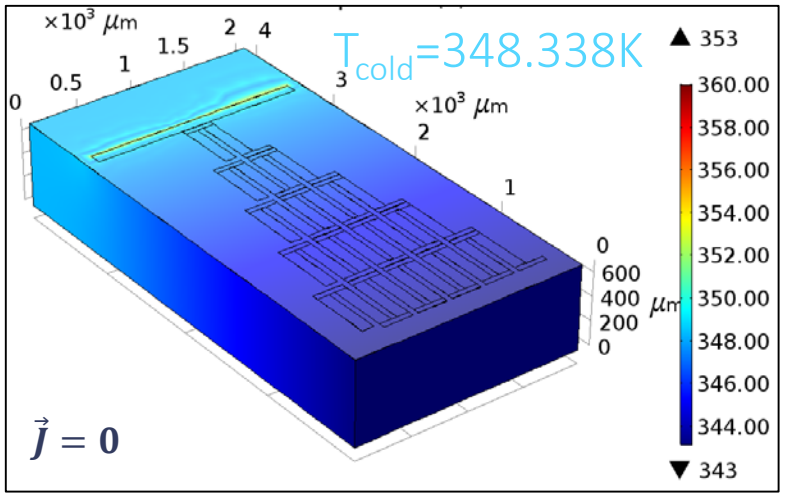


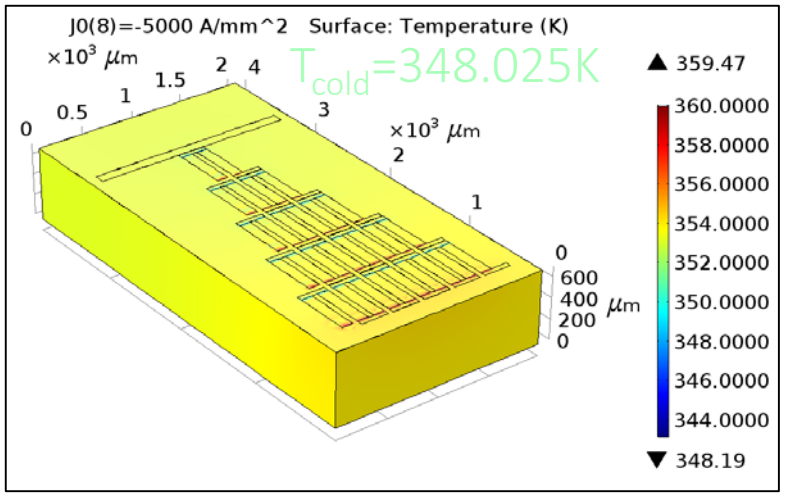
Max ΔT_{TEC}=353.15-348.025=**5.125K**

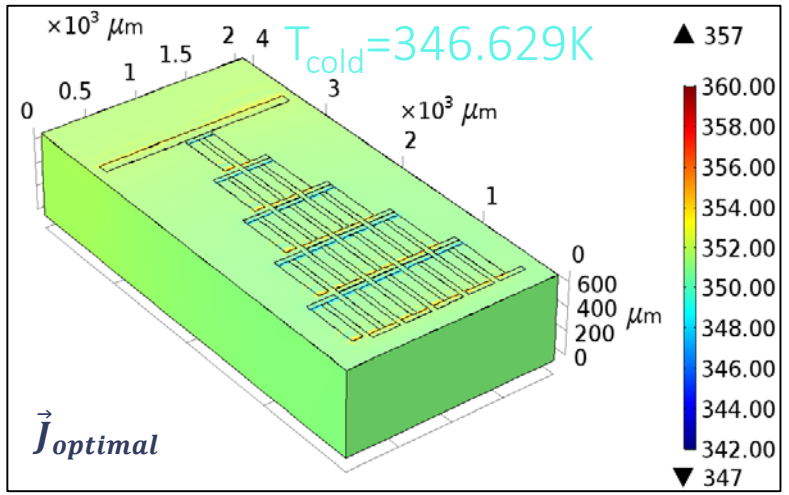
Lateral: Pyramidal Structure

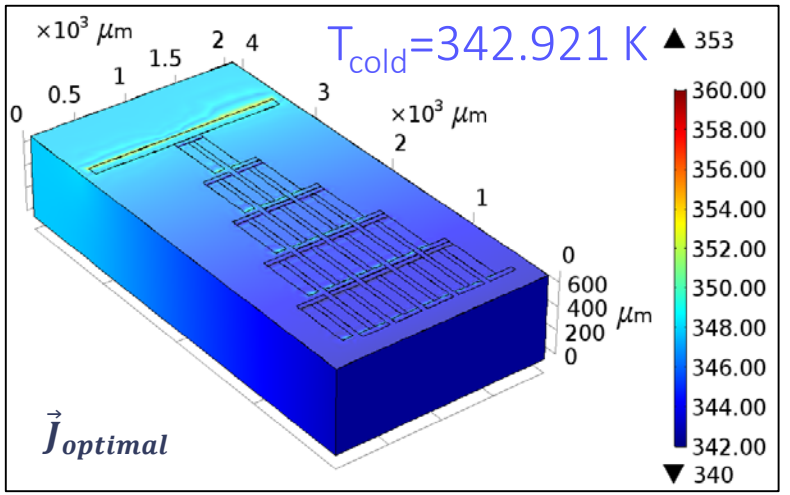












Max ΔT_{TEC}=5.125K

ΔT_{TEC}= 352.187 -346.629=5.558K

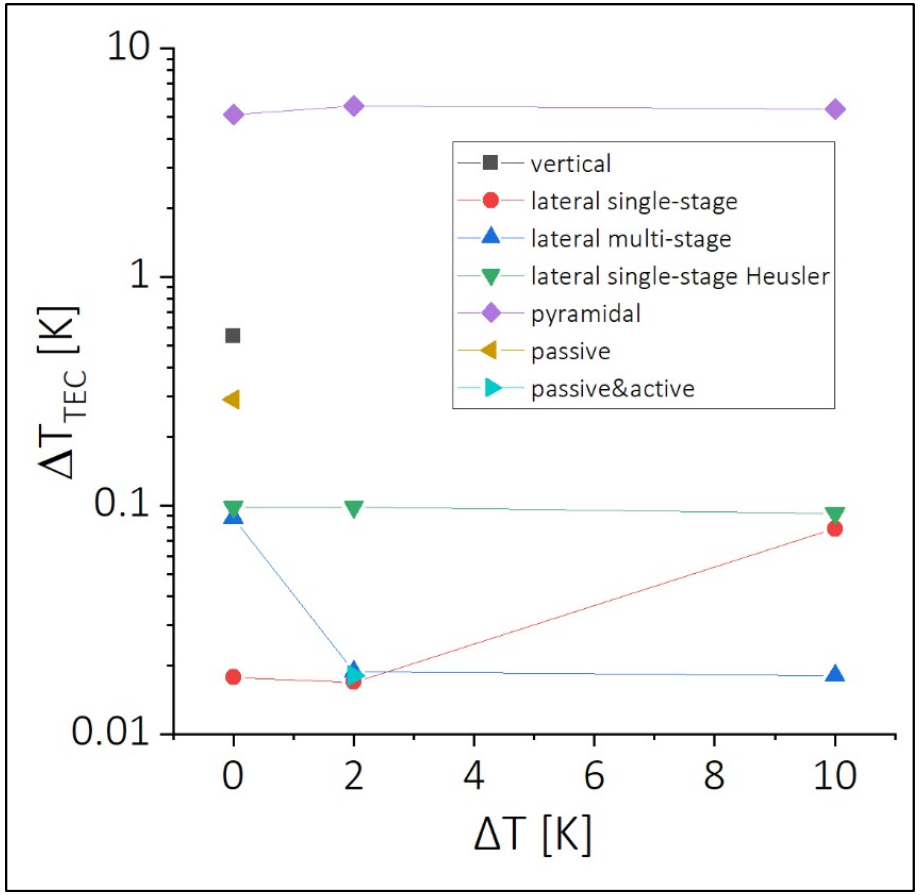
ΔT_{TEC}=348.338-342.921=5.417K

➡ pyramidal-TEC has significant impact on ΔT

Conclusion

- Lateral TECs → smaller influence than vertical TEC
- Lateral: $Fe_2V_{0.8}W_{0.2}Al$ has higher impact than poly-Si
- Passive cooling shows higher cooling effect than active & passive combination
- Pyramidal structure with poly-Si reach highest ΔT_{TEC}

➡ **further investigations of pyramidal structured TECs**



Thank you for your attention!

Questions?: caroline.schwinge@ipms.fraunhofer.de

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