ESSCIRC/ESSDERC 2020 Presentation
Power electronics trends 2025

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Outline

- Efficiency as a key driver for Power Electronics
- “Little box challenge”
- Pareto Front analysis in Power electronics
- Trends for efficiency and power density
- Conclusion

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(Power) Semiconductor drivers

Energy efficiency

Mobility

Security

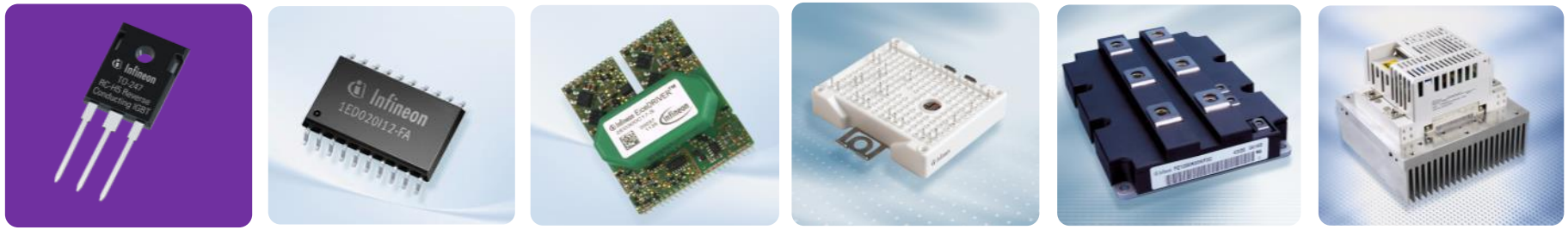
IoT & big data

Power Semiconductor drivers

Electrical energy supply chain

Energy generation | **Energy transmission** | **Energy consumption**

Power semiconductors

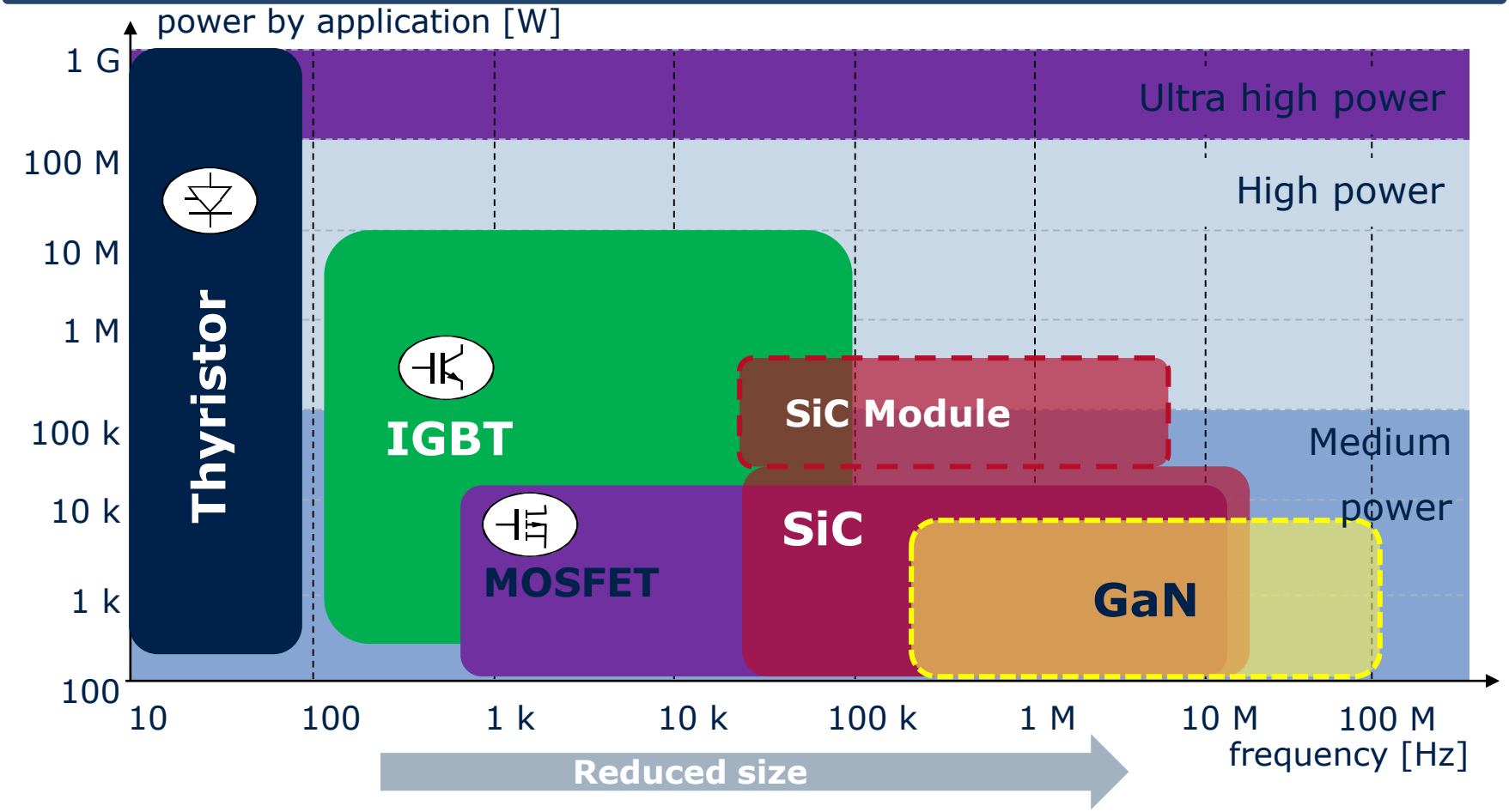


Power Switches

Application

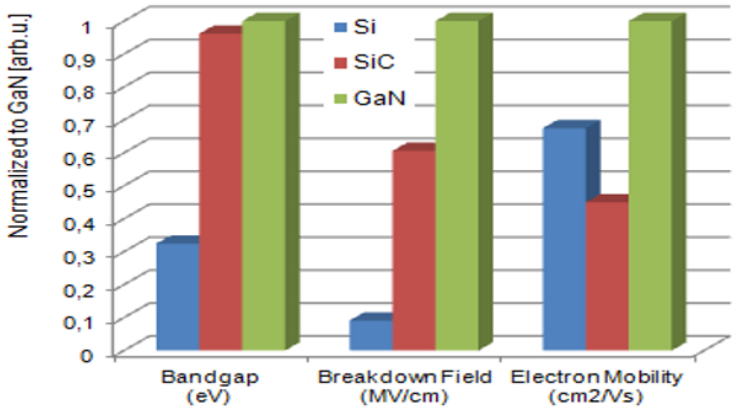
- HVDC
- High-current- supplies
- Large drives
- Ships
- Locomotives
- Large solar plants
- Trams, busses
- Electric cars
- On-roof PV
- Small drives
- Air conditioner
- Robotics
- Washing machine
- Switch mode power supplies

Future Scenario Powerelectronics

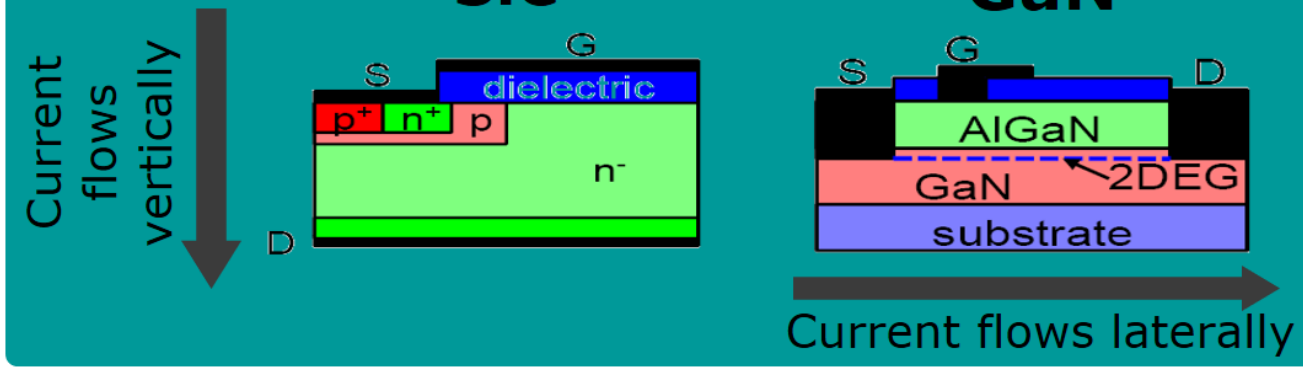


Material Properties

	Si	GaN	SiC
Band gap [eV]	1,1	3,4	3,2
Electron mobility [$cm^2/(V \cdot s)$]	~1.400	~2.200[a]	~900
Breakdown field strength [MV/cm]	0,3	3,4	3,2[b]
Reverse recovery charge [nC] Capacitive charge [nC]	~ 7000 ~ 250	"0" ~ 25	"0" ~ 30



Device concepts



- Even though GaN is a lateral device it achieves roughly same R_{on}*A (2mΩcm²) as SiC
- Only the lateral device opens new degrees of freedom for integration

[a] Mobility in the lateral 2DEG electron gas, bulk mobility is lower

[b] Based on recent in house measurements (publ. ISPSD 2014)

Classic Energy Distribution

Electricity Generation | **Transmission & Distribution** | **Consumption (example Notebook)**

Stone Coal power plant

AC-Transmission

Power Distribution

Power Supply

DC supply

Processor

60 W

Memory

Display

etc.

220 W
(ca. value)

90 W electricity

Mostly thermal losses

130 W (~60%)

1.4 W

3.6 W

13 W

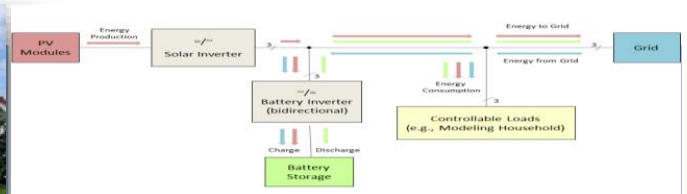
13 W

Electrical losses today : 31 W

Source: Infineon estimate

Sustainable Energy Flow

Electricity Generation | **Energy Storage** | **Consumption (example Notebook)**



Photovoltaic | Battery storage | DC/AC conversion | 90plus Power Supply | DC supply | Processor

84 W
(ca. value)

2 W | 5 W | 5 W | 5 W | 7 W | **60 W**

Memory, Display, etc

Losses: 24 W based on best in class Silicon

~12 W with GaN Technologies

Source: Infineon estimate

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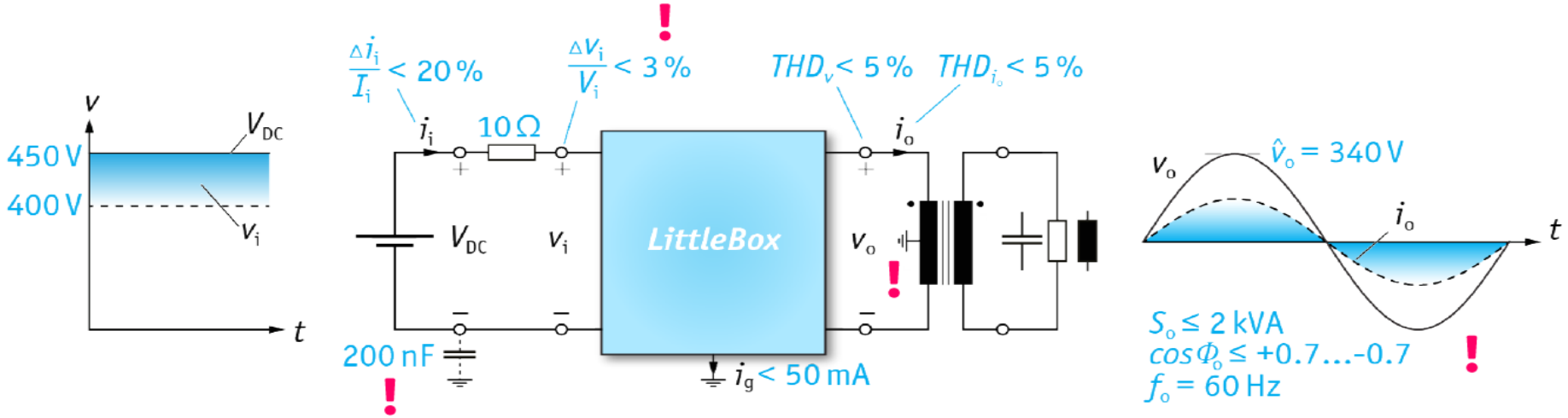
Little Box Challenge

LITTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



- Push the Forefront of New Technologies in R&D of High Power Density Inverters

Source: J.W. Kolar, CIPS 2016

Little Box Challenge

The Grand Prize

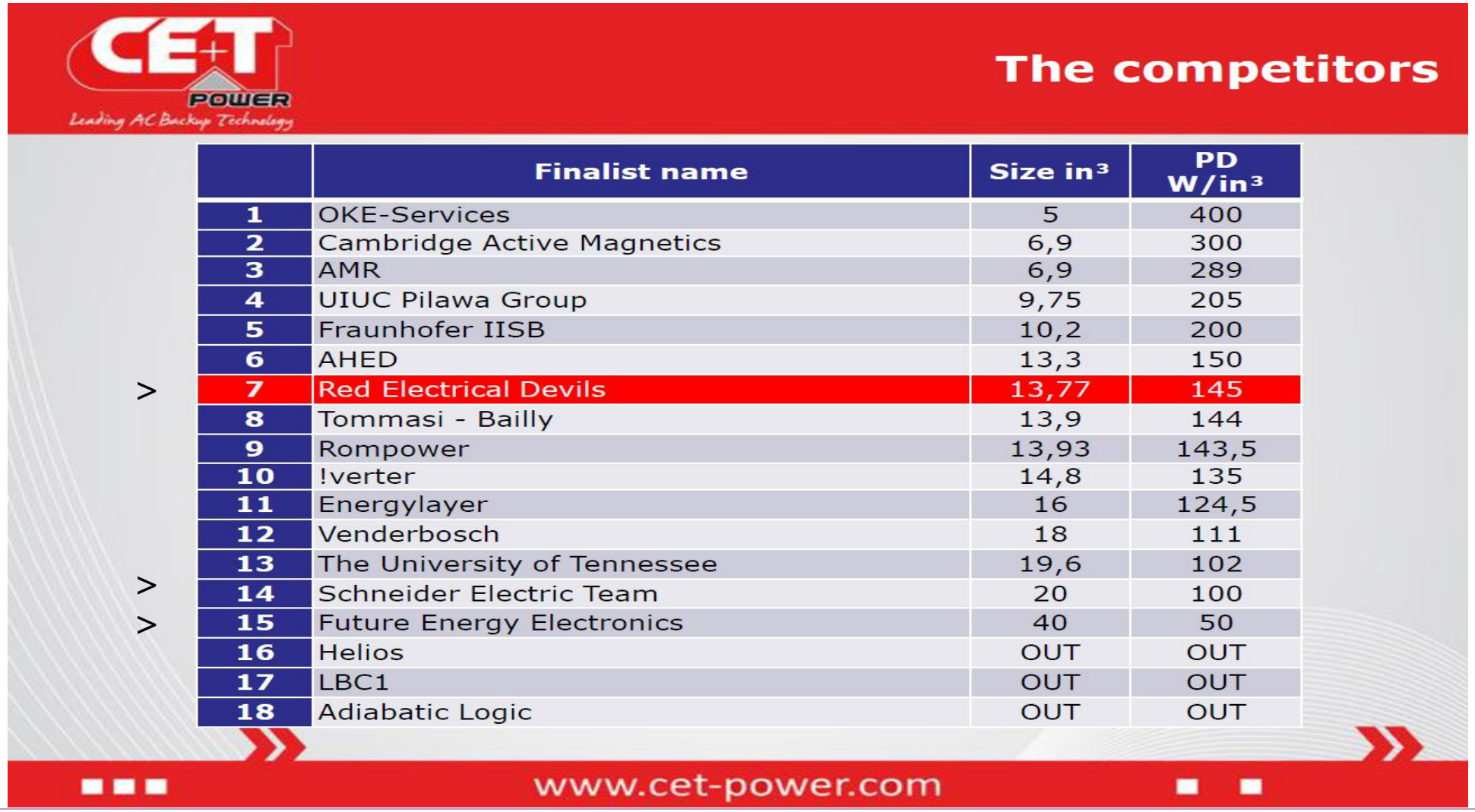
- Highest Power Density (> 50W/in^3)
- Highest Level of Innovation

$1,000,000

- **Timeline**
  - Challenge Announced in Summer 2014
  - 2000+ Teams Registered Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - 18 Finalists (3 No-Shows)

Source: J.W. Kolar, CIPS 2016

3 Survivals after 100h Test



		Finalist name	Size in³	PD W/in³
	1	OKE-Services	5	400
	2	Cambridge Active Magnetics	6,9	300
	3	AMR	6,9	289
	4	UIUC Pilawa Group	9,75	205
	5	Fraunhofer IISB	10,2	200
	6	AHED	13,3	150
>	7	Red Electrical Devils	13,77	145
	8	Tommasi - Bailly	13,9	144
	9	Rompower	13,93	143,5
	10	!verter	14,8	135
	11	Energylayer	16	124,5
	12	Venderbosch	18	111
	13	The University of Tennessee	19,6	102
>	14	Schneider Electric Team	20	100
>	15	Future Energy Electronics	40	50
	16	Helios	OUT	OUT
	17	LBC1	OUT	OUT
	18	Adiabatic Logic	OUT	OUT

Winner application

CE+T POWER
Leading AC Backup Technology

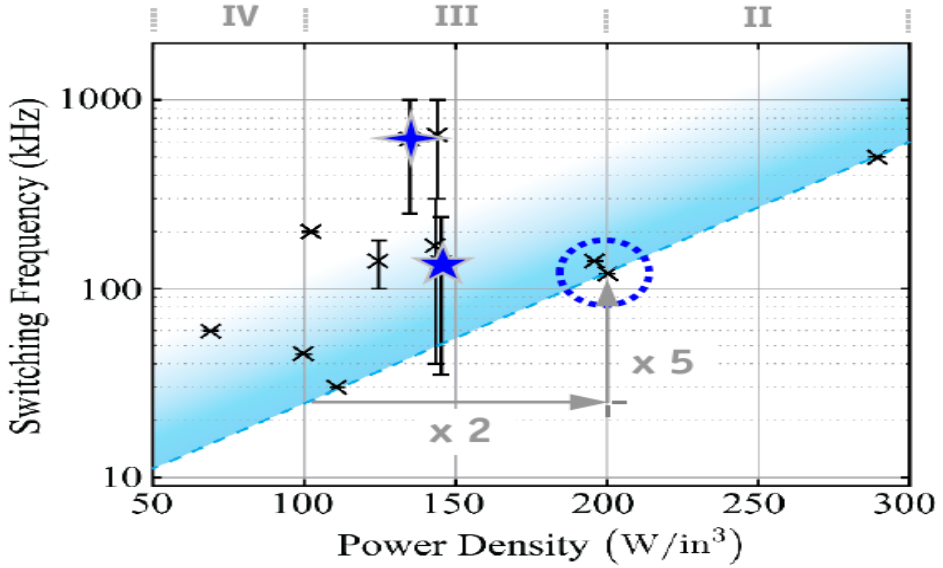
Result

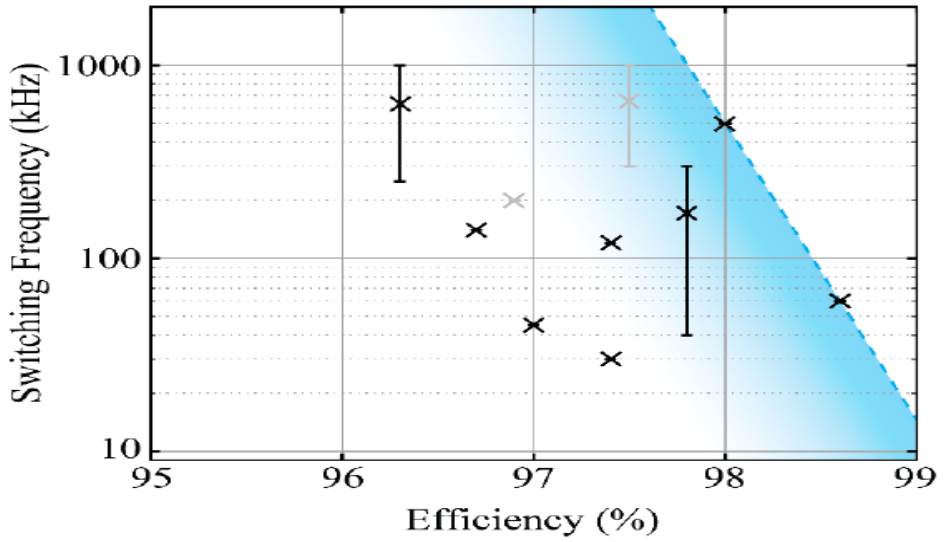
www.cet-power.com

WBG enabled system benefits

Finalists – Performance Overview

- 18 Finalists (3 No-Shows)
- 7 Groups of Consultants / 7 Companies / 4 Universities





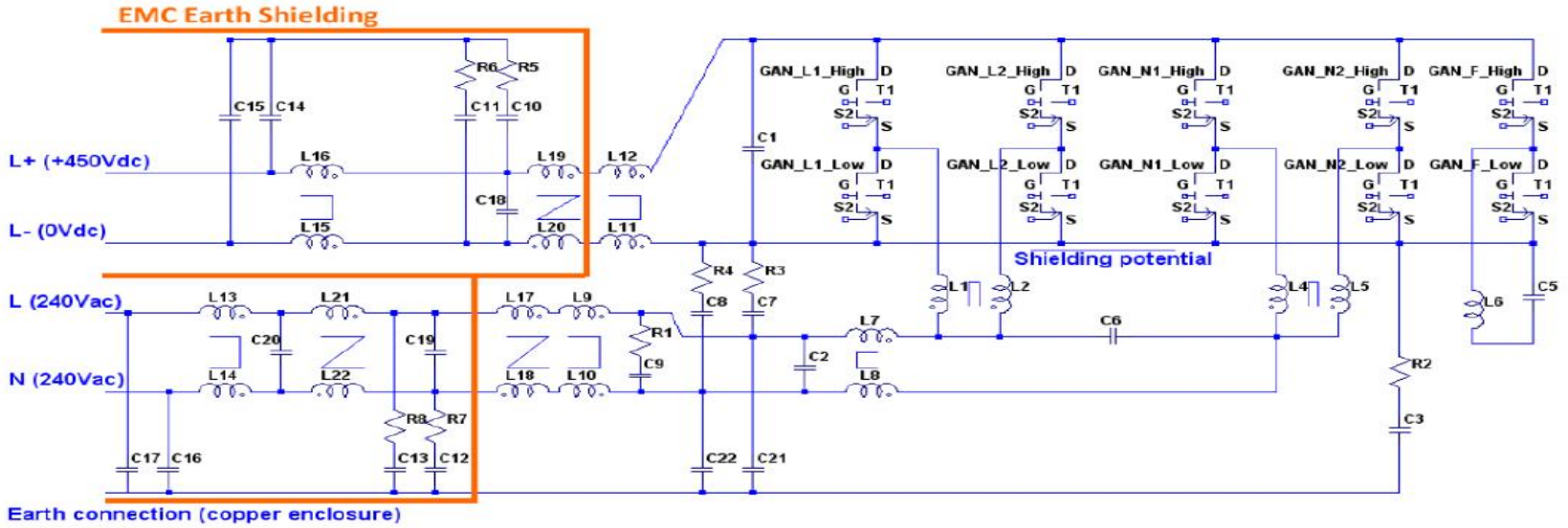
- 70…300 W/in³
- 35 kHz…500kHz…1 MHz (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC| Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)

Source: J.W. Kolar, CIPS 2016

WBG enabled system benefits

Category III: 100 – 200 W/in³ (8 Teams) – Example

- "Advanced Industrial"
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Frequ. Common-Mode AC Output Component



- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150µF)

Source: J.W. Kolar, CIPS 2016

WBG enabled system benefits

Conclusions

- There's **NO** Silver Bullet .... **BUT** a Set of Core Concepts & Technologie

- >200W/in³ (12kW/dm³) Achievable
- f_s < 150kHz (Constant) Sufficient
- SiC Can Also Do It
- ZVS (Partial) Helps
- Full-Bridge Output Stage
- Active Power Pulsation Buffer (Buck-Type, X6S Cap.)
- Conv. EMI Filter Structure
- Multi-Airgap Litz Wire Inductors
- DSP Can Do It (No FPGA)
- Careful Heat Management (Adv. Heat Sink, Heat Distrib., 2-Side Integr. Cooling, etc.)
- Careful Mechanical Design (3D-CAD, Single PCB, Avoid Connectors, etc.)

Overall Summary

- No (Fundamentally) New Approach
- Passives & 3D-Packaging are Finally Defining the Power Density → **CIPS (!)**
- Competition Timeframe Too Short for Advanced Integration
- Building a Full System Not Possible for Many Universities – High Drop Out Rate

Source: J.W. Kolar, CIPS 2016

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Multi-objective Optimization

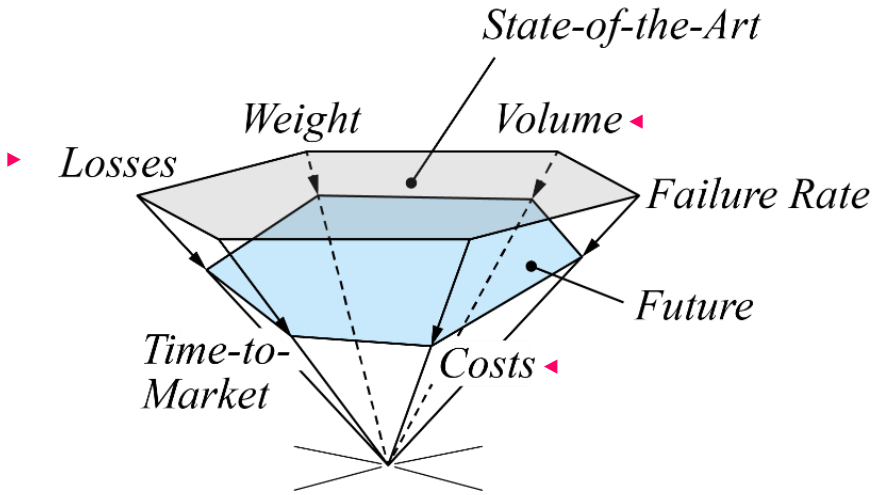
- Customers typically Demand Improvements of Power Electronic Systems in Multiple Dimensions, e.g.

More Efficient and Cheaper!

More Efficient and Smaller at Same Cost!

Smaller and Cheaper!

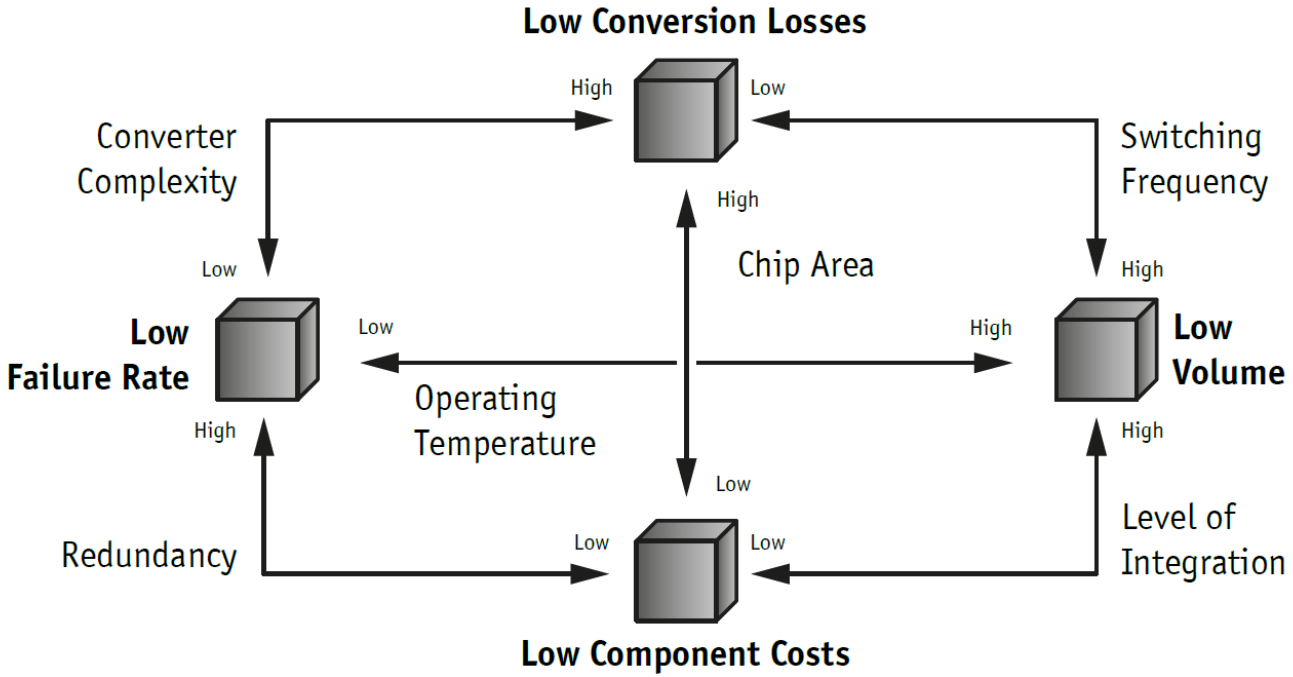
- Today's Analysis and Design Methodologies
  - Single-Objective Optimization (e.g. Efficiency OR Power Density)
  - No Cost Considerations
  - Non-Systematic Hardware Prototyping



Source: M. Kasper, ETH-PES 2017

Design Challenges

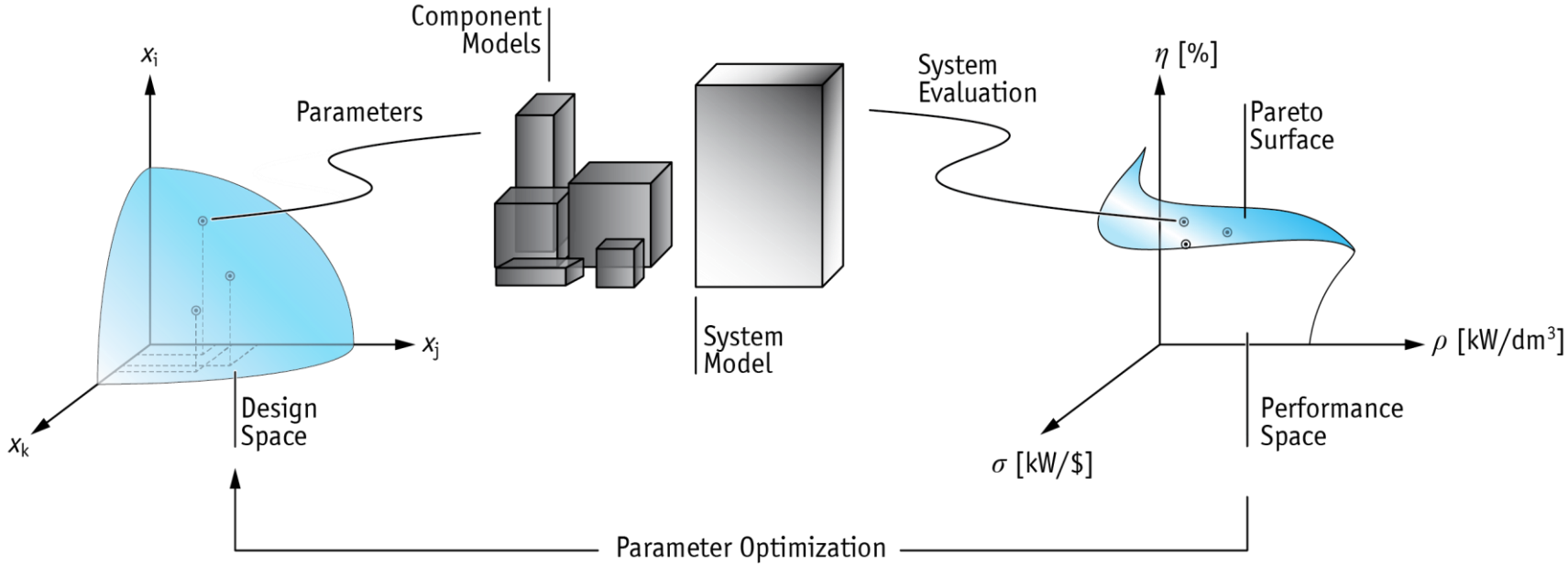
- Large Number of Degrees of Freedom
  Topology, modulation scheme, switching frequency, semiconductor technology, inductor design, etc.
- Mutual Coupling of Performance Indices



Systematic Multi-Objective Design Approach Required which Considers All Available Degrees of Freedom

Source: M. Kasper, ETH-PES 2017

Virtual Prototyping Design



- Systematic Approach
- Comprehensive and Detailed Modeling
- Multi-Objective Pareto Optimization
- Consideration of Efficiency, Volume (Weight), and Costs

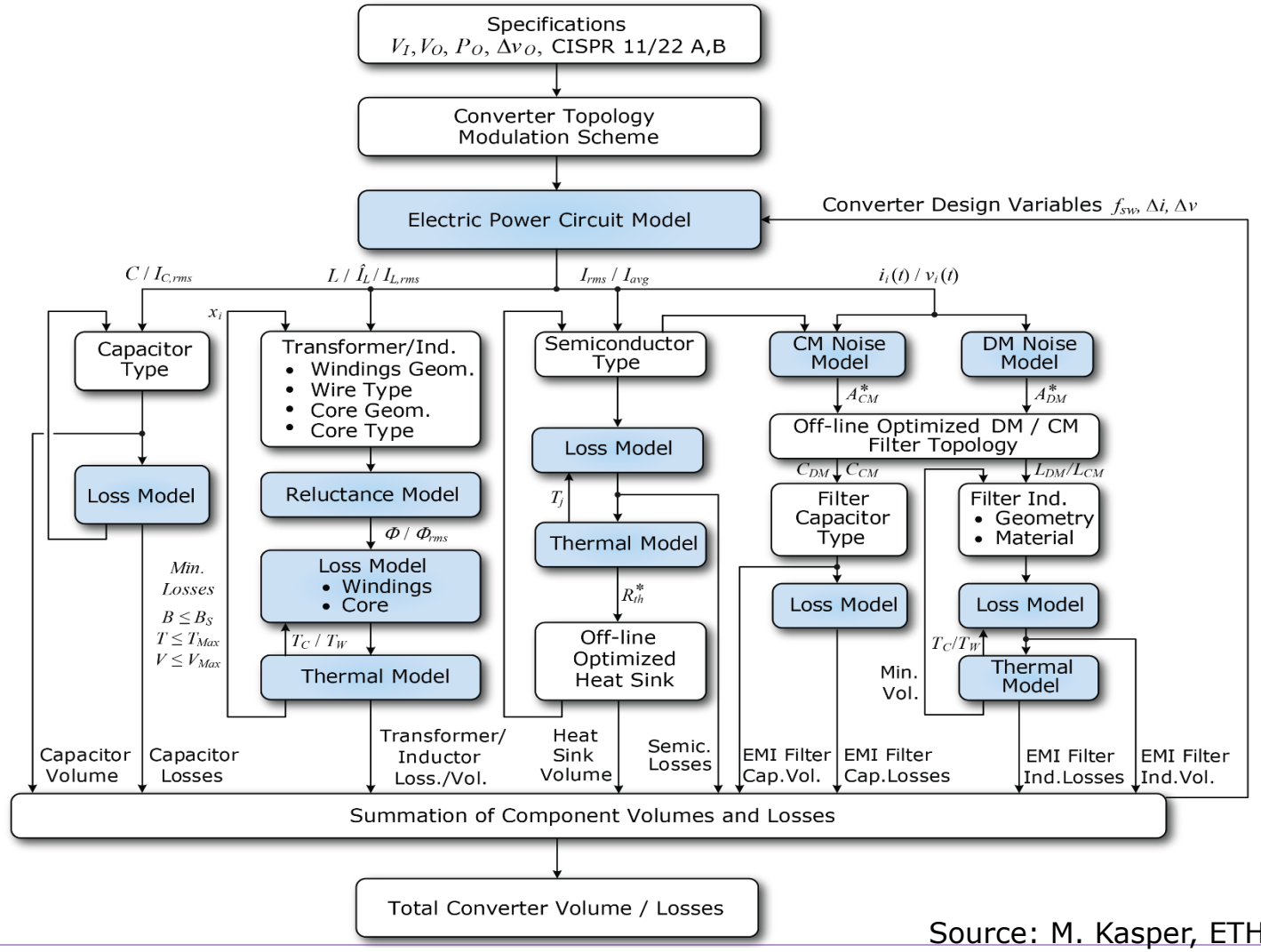
Source: M. Kasper, ETH-PES 2017

Mathematical Modeling

System Level

Component Level

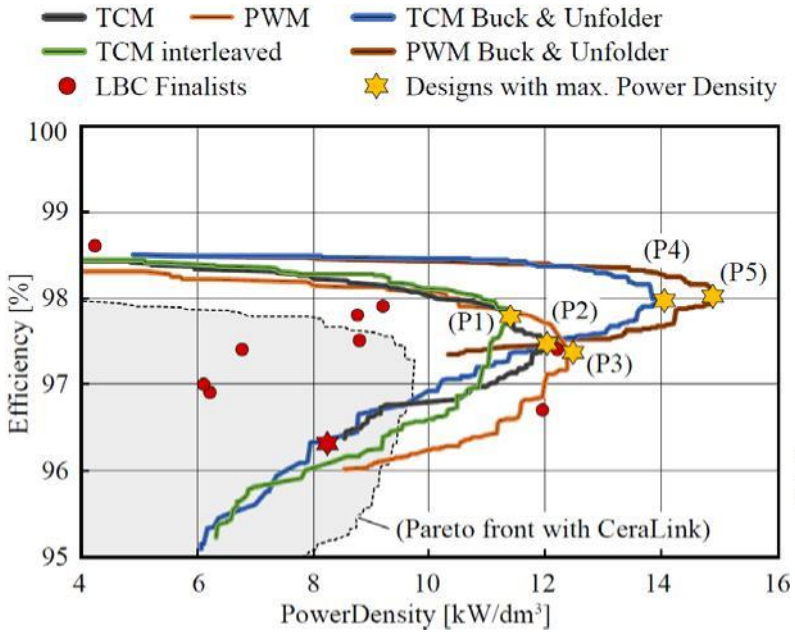
System Level



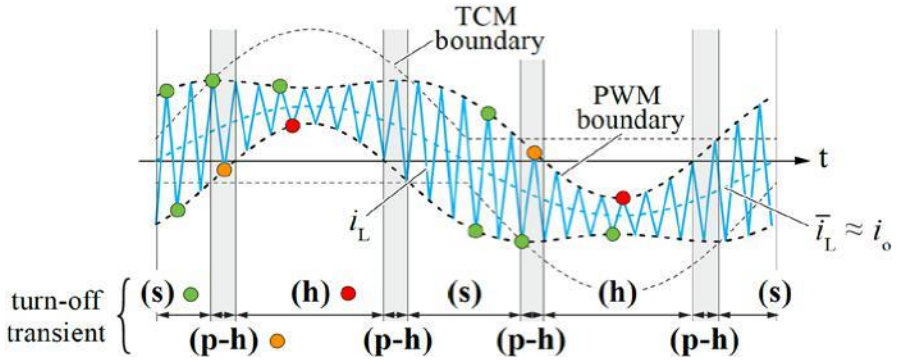
Source: M. Kasper, ETH-PES 2017

Pareto Front "Little Box 2.0"

- DC/|AC| - Buck Converter (Single Bridge Leg) + Unfolder & PWM Shows Best Performance
- Full-Bridge Would Employ 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. but Larger Total Vol. of Switches and Inductors



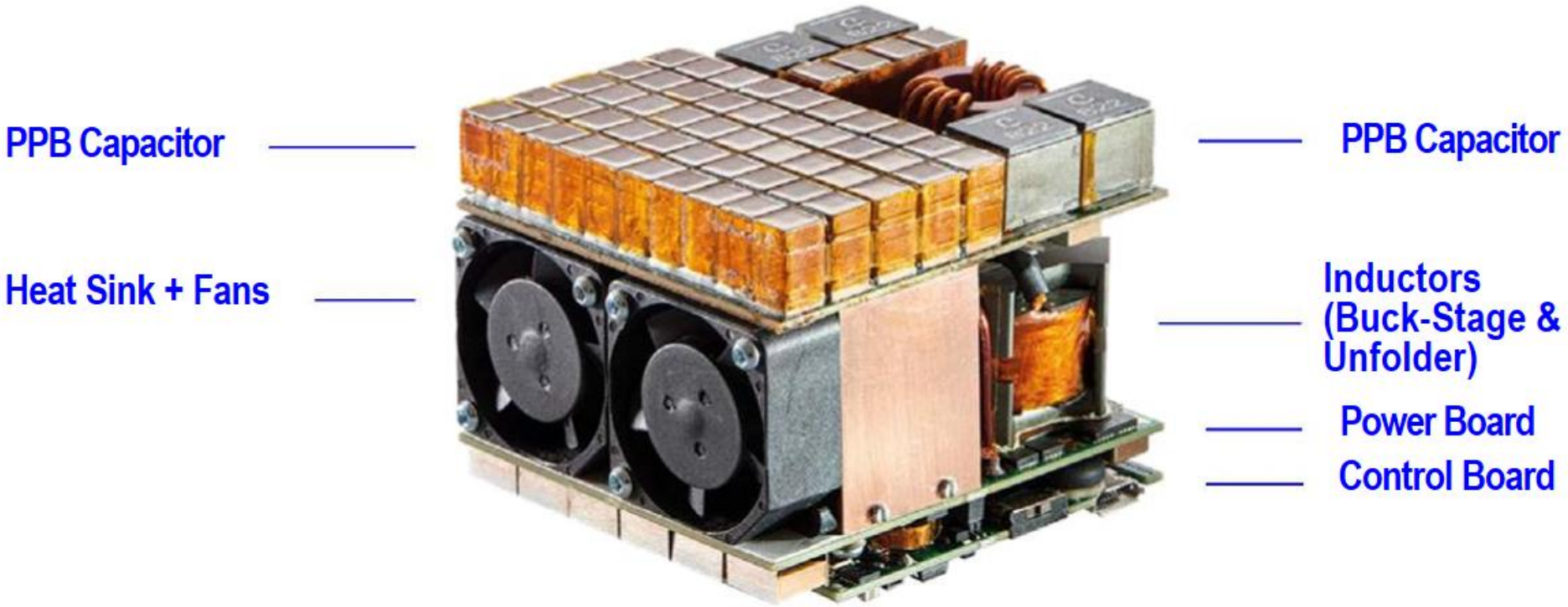
(s) Soft-Switching (ZVS)
(p-h) Partial Hard Switching
(h) Hard-Switching



■ ρ= 250W/in³ (15kW/dm³) @ η= 98% Efficiency Achievable for Full Optimization

Source: D. Neumayr, SCAPE 2019

Little Box 2.0 Demonstrator



- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Source: D. Neumayr, SCAPE 2019

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Trends for power density

- Power densities have to be compared **only** within **one kind of system** (in this talk forced air cooling for systems in the range of 2 kW were discussed)
- Values for systems with water cooling or non forced cooling are completely different
- In terms of power density research is far ahead of industrial systems because of long term reliability and cost issues
  - For example: Little Box winner showed 145 W/in³ in **2015**
  - Best industrial use case **today** shows up with about 70 W/in³

➔ Expectation: in 2025 up to 120 W/in³ could be feasible in industry and about proven 300 W/in³ in research

Trends for efficiency

- Also efficiencies are varying between different **kinds of systems and applications**
- For PV (Photovoltaic) inverters peak efficiencies up to 99,3% were already demonstrated 10 years ago.
- Efficiencies in industrial systems are steadily improving driven by sustainability and CoO (Cost of Ownership) reasons
  - For example: Commercial PV-Inverters today are offered with efficiencies between 97% and 98%
  - Best OBCs (On Board Chargers) are around 96%

➔ Expectation: in 2025 I would expect PV-inverters still in the lead for efficiencies in industry in the range between 98% and 99%

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Conclusion

- Power density and efficiency are innovation drivers for Power Semiconductors
- Especially GaN (GalliumNitride) and SiC (Silicon Carbide) technologies are of interest when volume and weight is a value
- Higher efficiencies are driven by sustainability and CoO (Cost of Ownership) reasons and at least by legal requirements

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